

From Beams to Bits: Real-Time AI Engines for Particle Physics

Shih-Chieh Hsu
University of Washington



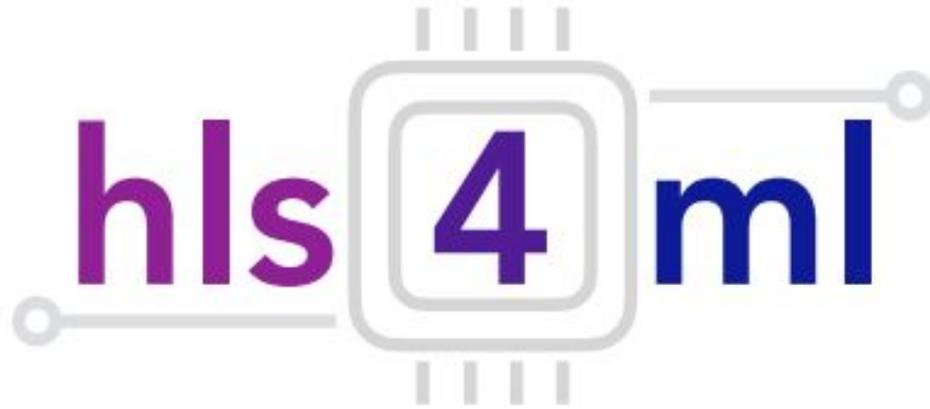
PHY-2117997

Mar 9 2026

ICEPP, University of Tokyo

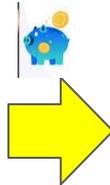


<https://a3d3.ai/>

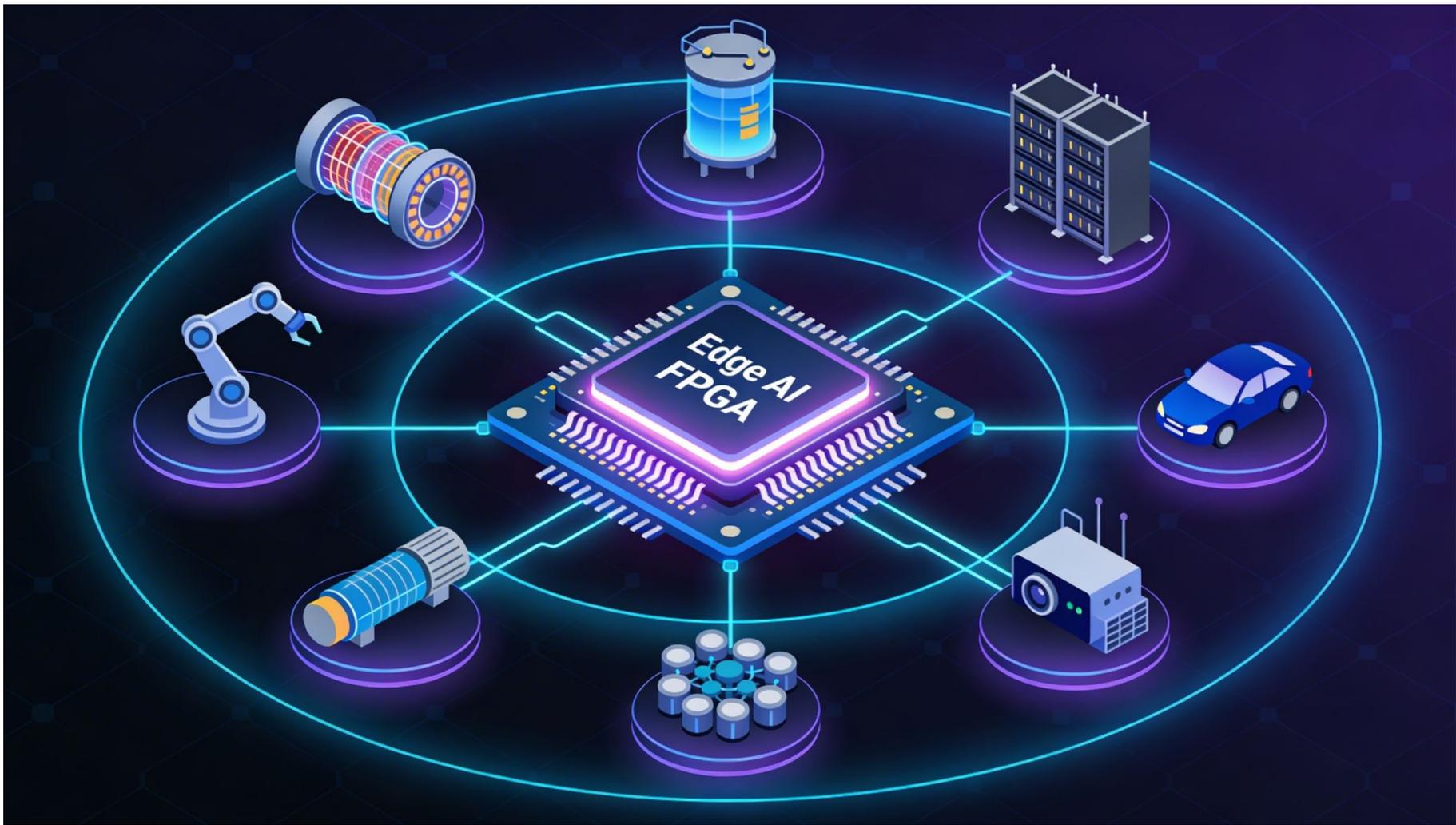


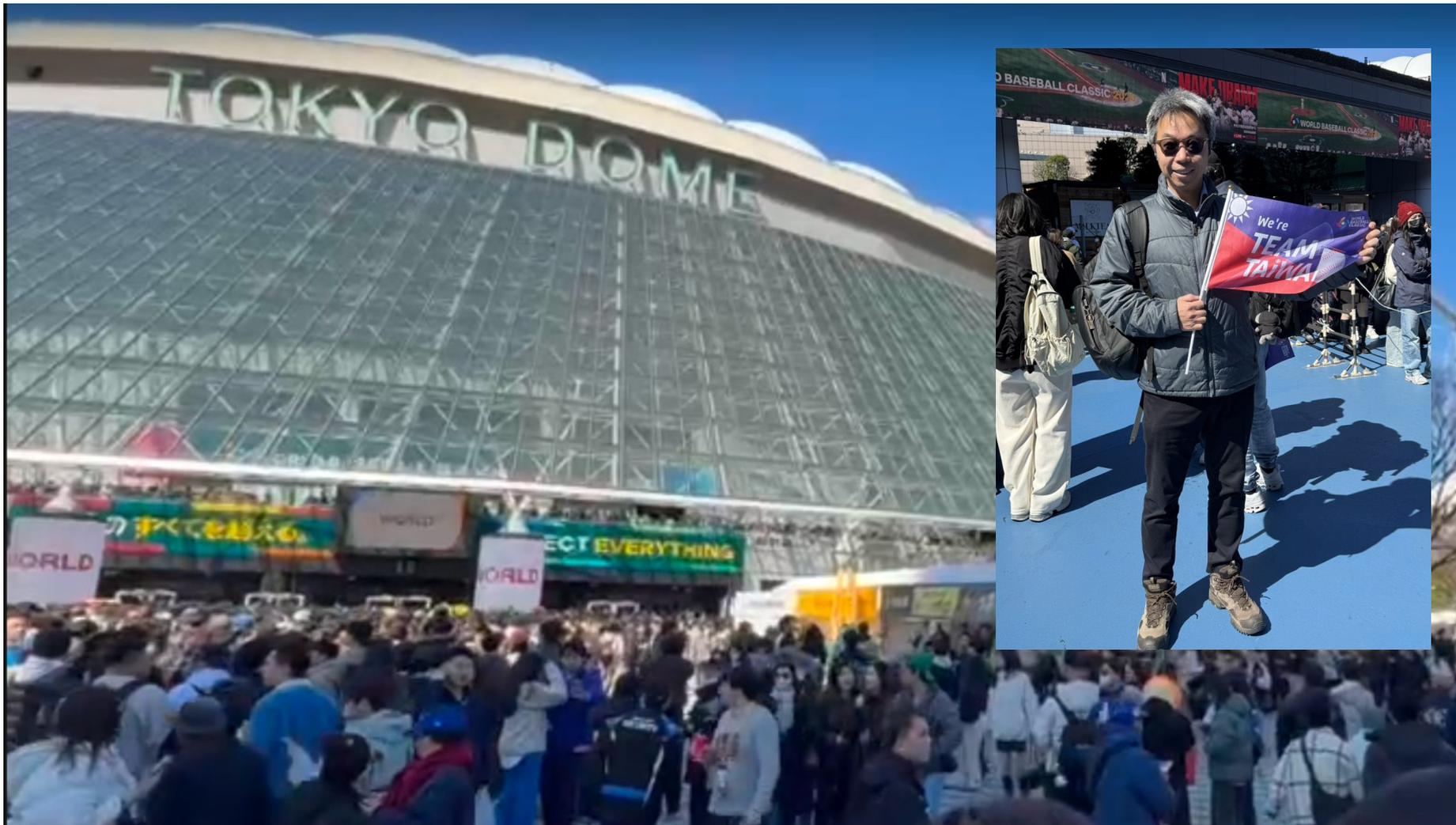
Open-source Python package that **converts** trained ML models (Keras, PyTorch, ONNX, etc.) into FPGA/ASIC firmware via **high-level synthesis** for low-latency inference

1 FPGA engineer + 0.3 FTE ML engineer.
3 months



0.3 FTE ML engineer (no HDL experiences).
5 day







Shih-Chieh (Jay) Hsu

徐士傑

- Professor, University of Washington Physics
- Adjunct Professor, University of Washington Electrical and Computer Engineering
- Adjunct Professor, National Tsing Hua University Physics
- Director, NSF HDR Institute A3D3
- Vice President, National Taiwan University Alumni Association of Northwest America
- Vice President, North America Taiwanese Science and Engineering Association, Seattle Chapter

<https://www.linkedin.com/in/shih-chieh-hsu-hep/>
<https://www.facebook.com/schsupy>



Dr. Hsu studies studies
fundamental science
using real-time AI.



schsu@uw.edu

2025
**U.S. Taiwan
 Tech
 Connect**
 AI Trends &
 Industry Insights

NATEA SEATTLE



Ethan Tu
 Founder & CEO
 Taiwan AI Lab



Elaine Lu
 VP of Engineering Operations
 CoreWeave



Shyam Gollakota
 Professor of CS, UW
 Co-founder of Hearsay AI



Kwok Cheung
 Founder & CEO
 KC-Excellia Consulting

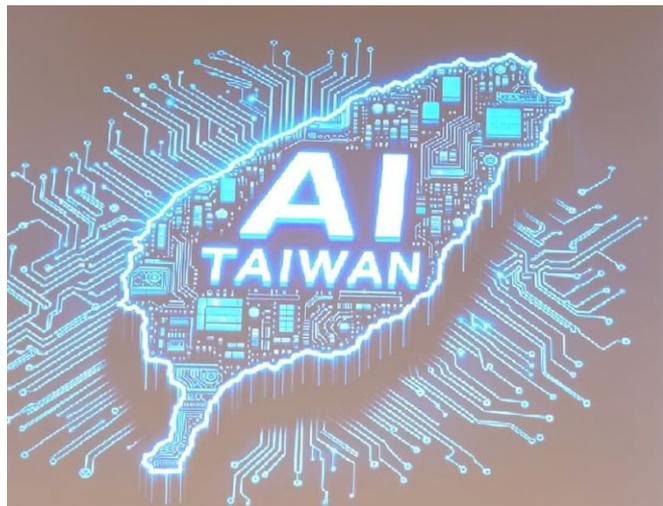


Miriam Teng
 Principal Accounting
 Manager, Amazon

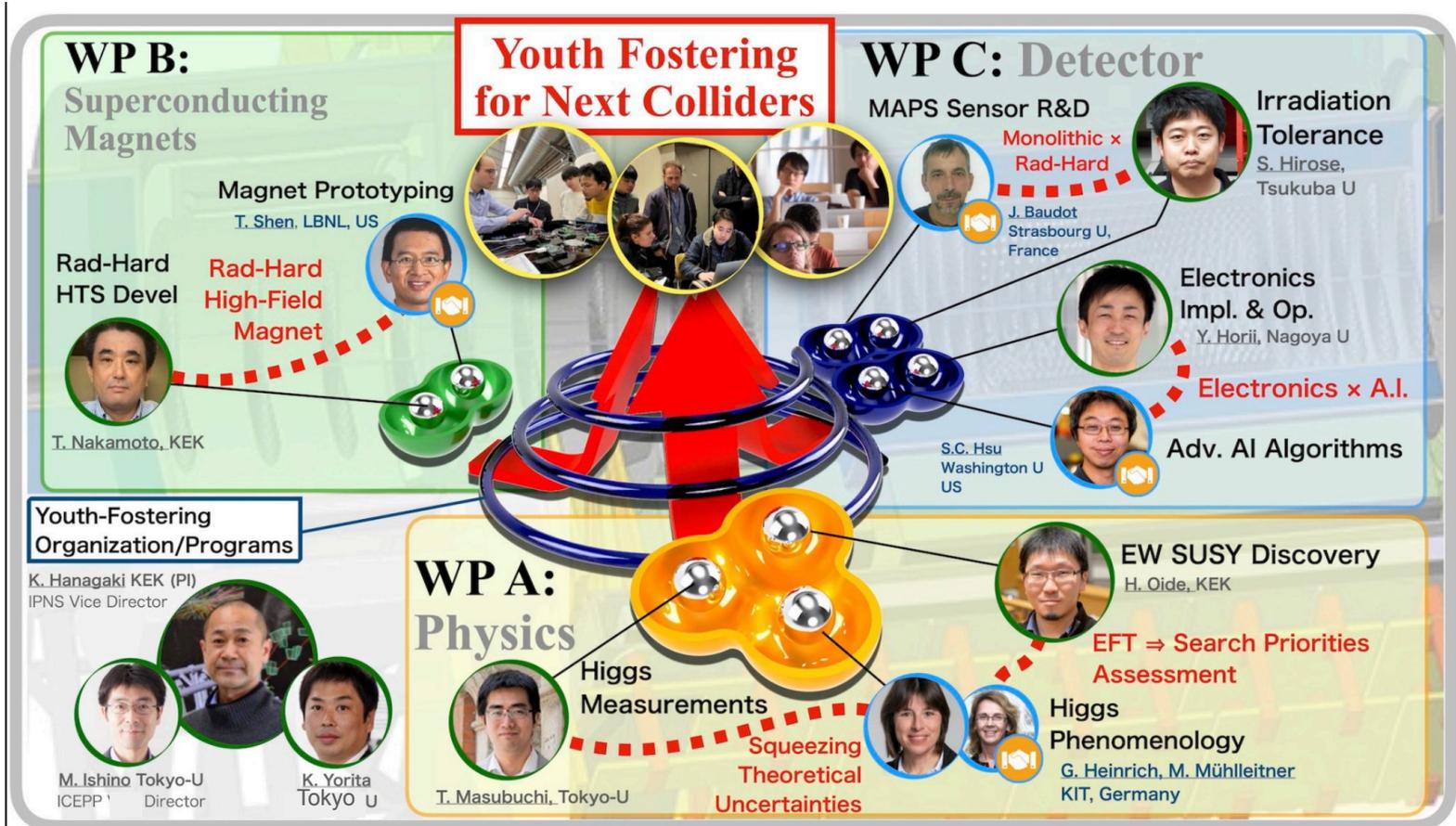


Hubert Tsai
 Founder & CTO
 Chieuro

Nov 15th at UW
 Scan to register

Introduction/Advertisement of International Leading Research (JSPS grant) Development of the Energy Frontier and International Human Resources toward Unified Understanding of Interaction



Real-Time Adaptive AI for Sleep Diagnosis, Treatment and Therapy Cross-Pacific Initiative (X-PAI)



Dr. Shih-Chieh Hsu (PI)
Professor of Physics
Director of A3D3



Dr. Scott Hauck
Professor of ECE



Dr. Amy Orsborn
Professor of ECE/BioEng



Dr. Eli Shlizerman
Professor of ECE/AMath

NSF HDR Institute A3D3, University of Washington



Dr. Shun Nakajima (PI)
Associate professor

Dr. Kei Muroi, MSc. Shio Maeda, MSc. Hiroku Noma
Dr. Azusa Ishii

International Institute for Integrative Sleep Medicine
University of Tsukuba



Dr. Hiroyuki Kitagawa
Professor



Gifu Mates Sleep Clinic
Sleep Medicine Specialist

Dr. Haruhito Tanaka (Physician)

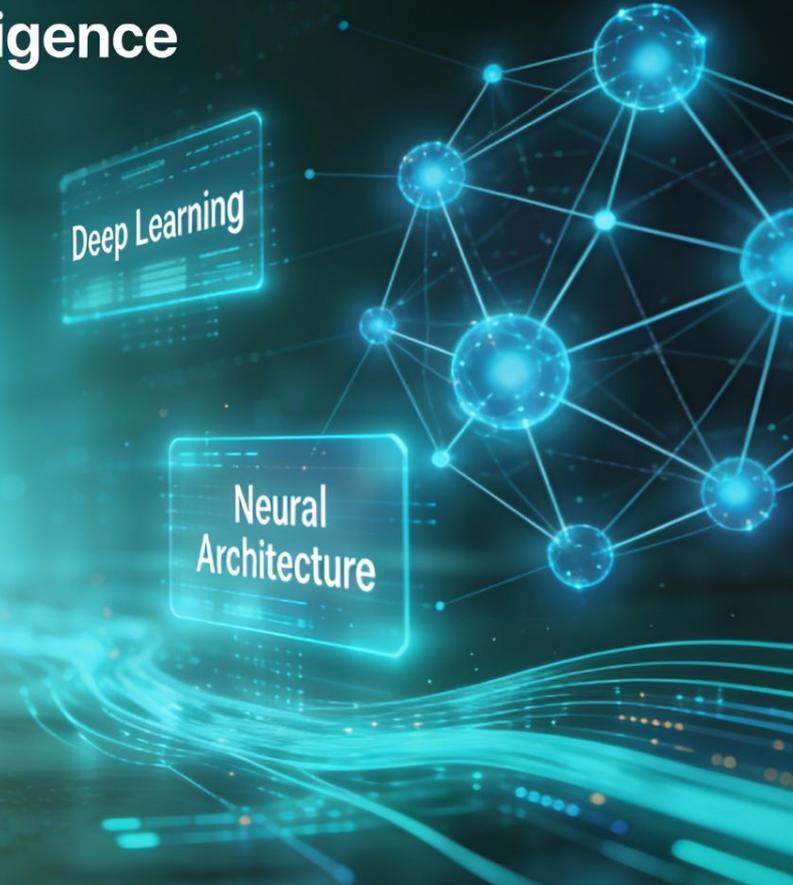
Hiroaki Yamamoto
(Registered Polysomnographic Technologist)

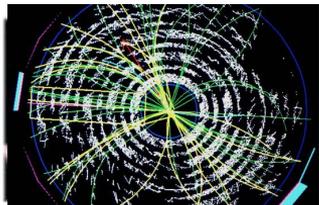
Convergence of Traditional Science and Artificial Intelligence



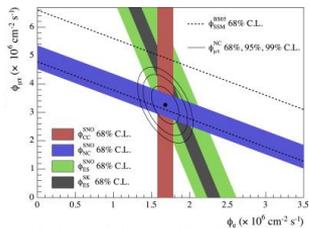
Deep Learning

Neural
Architecture

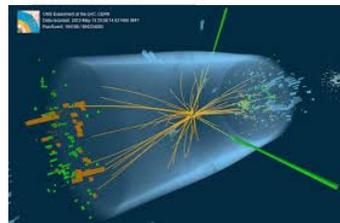




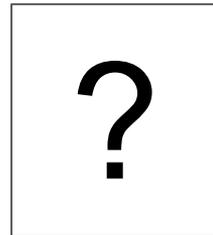
Top discovery
1995



Neutrino Oscillations
2001



Higgs Discovery
2012



1995
Support Vector Machine

2001
Gradient Boosting

2012
AexNet

2016
AlphaGo

2020
AlphaFold

2022
ChatGPT

2024
Agentic AI

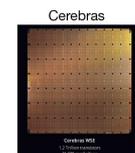
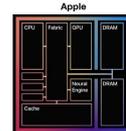
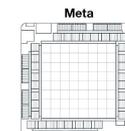
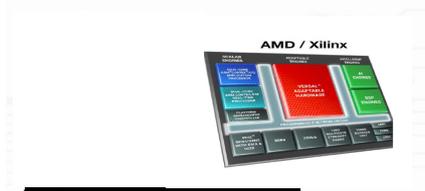
Deep Learning
revolution

GenAI
revolution

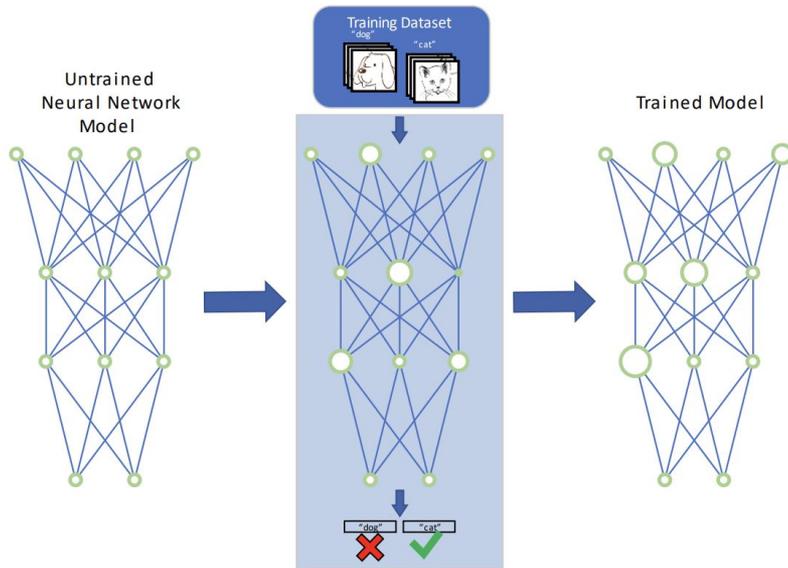
Trending in industry



Advances driven by
big data explosion
& machine learning

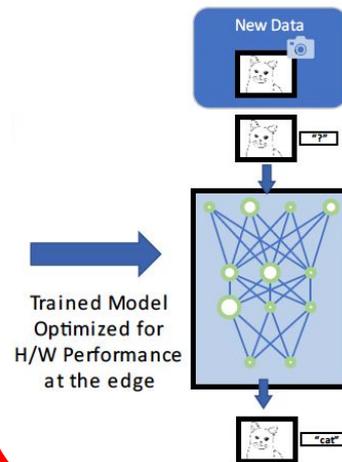


Training



- Very large datasets & memory, CPU/GPU/TPU farms, floating point required
- Done in an AI/ML Framework (Tensorflow, PyTorch, etc.).

Inference

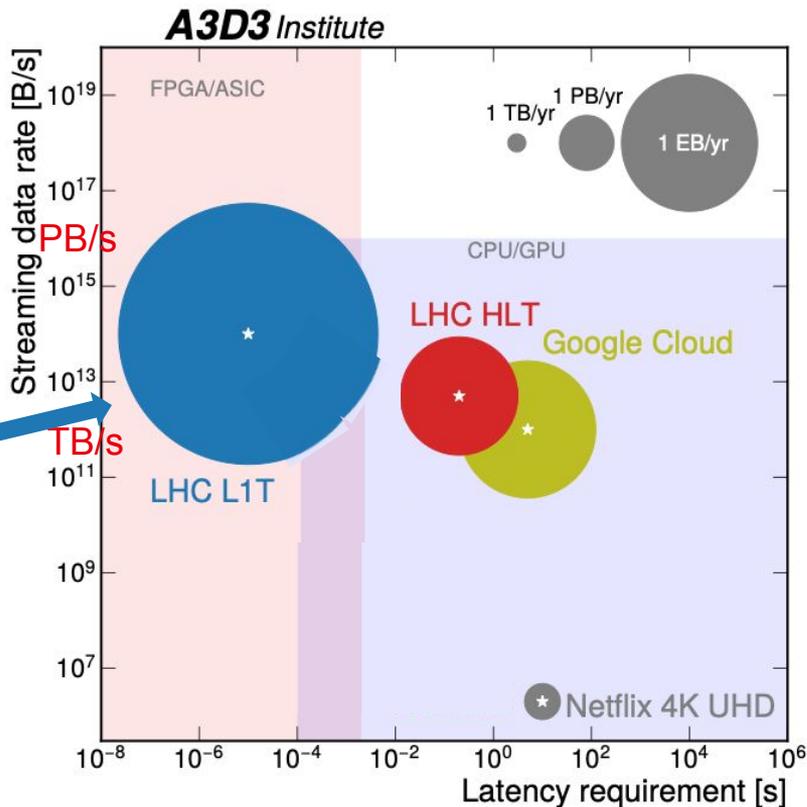


Focus
of this
talk

- Requires minimal computational resources
- Often has real-time performance/power requirements that require custom hardware, e.g. FPGA/ASIC/Edge devices

LHC pushes technology limits

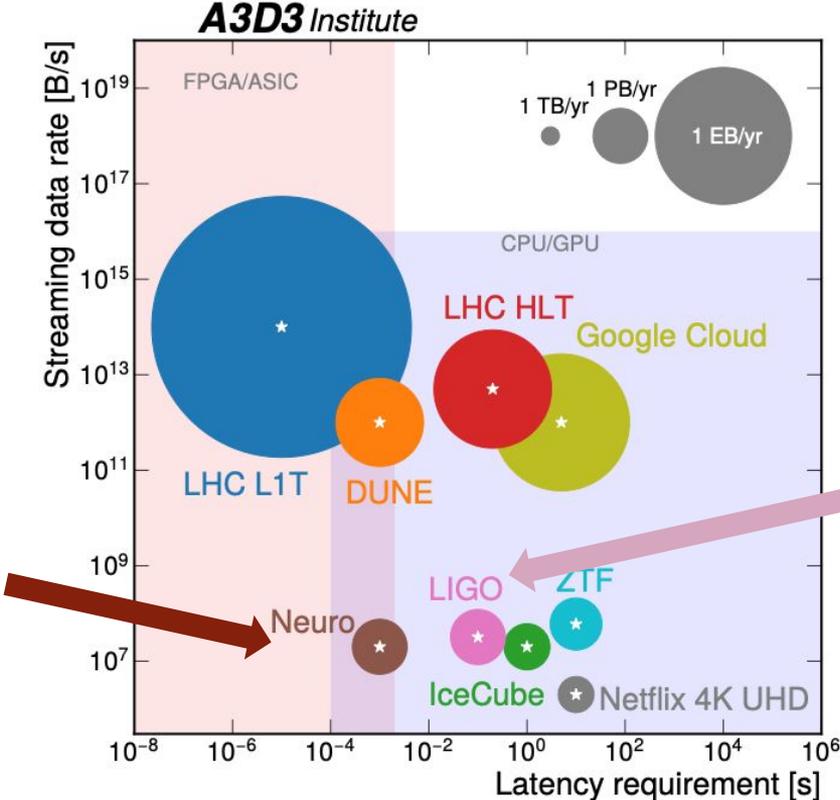
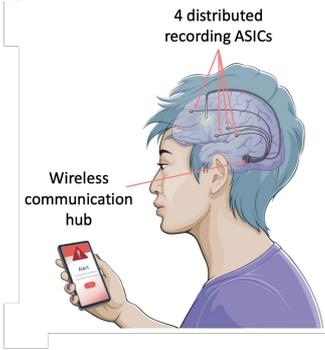
High Energy Physics



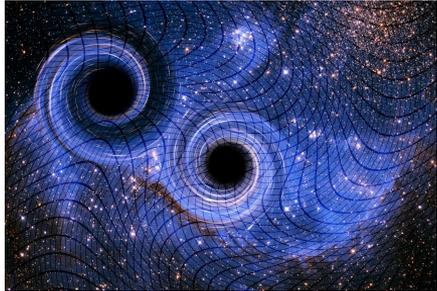
- **Data volumes** surpass industry standards
- **Streaming rates** exceed commercial benchmarks

Critical Common challenges

Neuroscience



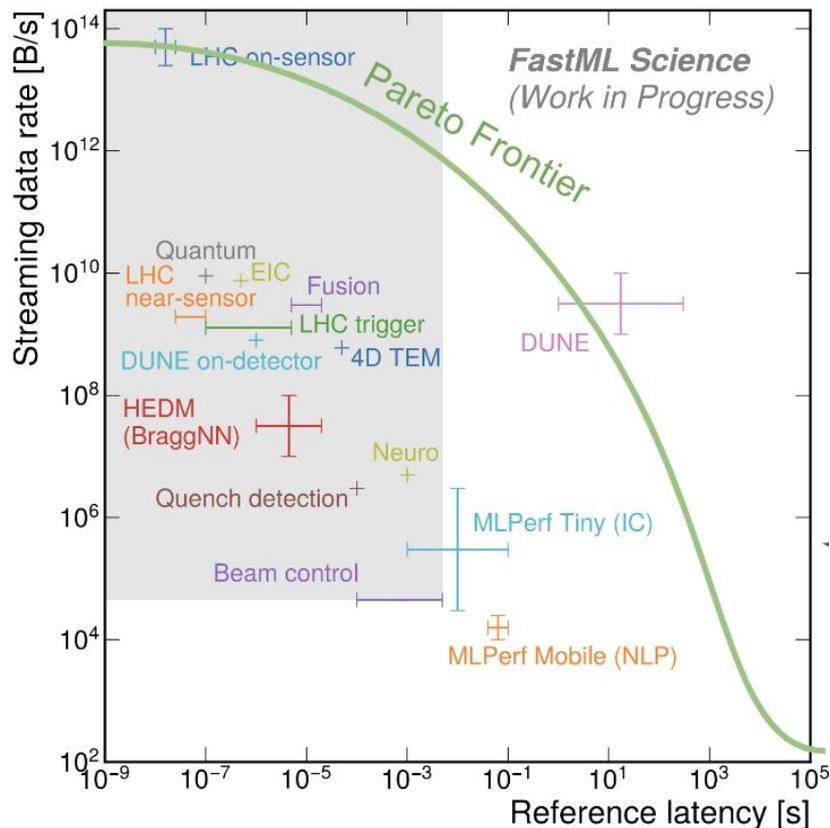
Gravitational Wave



Fast Machine Learning Community

High-performance data systems with

- low latency
- high throughput processing,
- real-time control modules, and
- custom processing elements.



Fast Machine Learning Community

High-performance data systems with

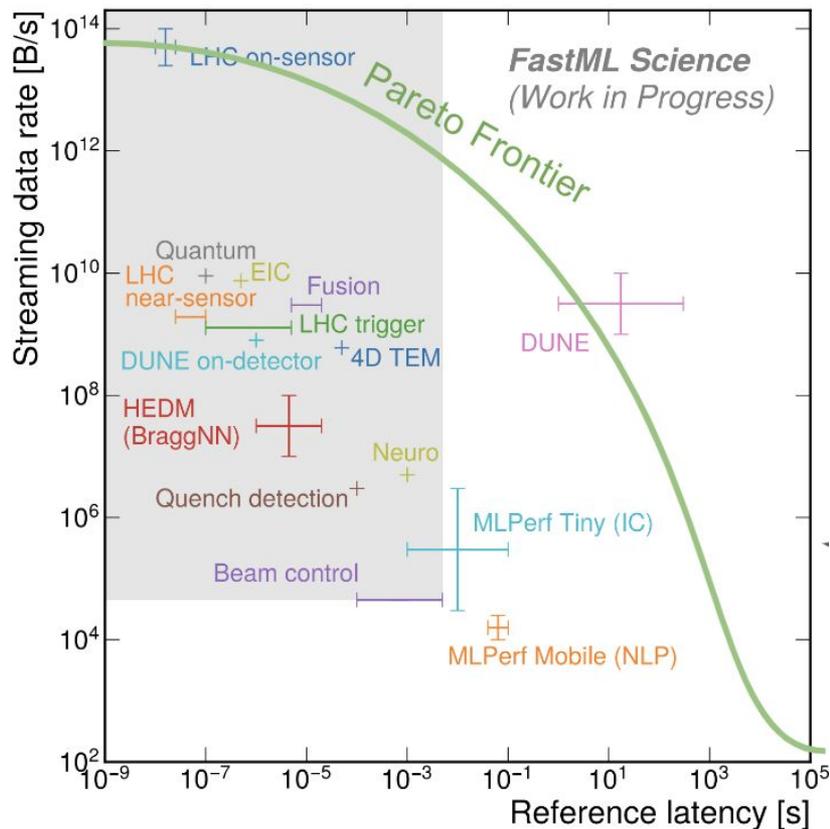
- low latency
- high throughput processing,
- real-time control modules, and
- custom processing elements.



pose-hls4ml
EPIGRAPHY



NextGen
Next Generation Triggers





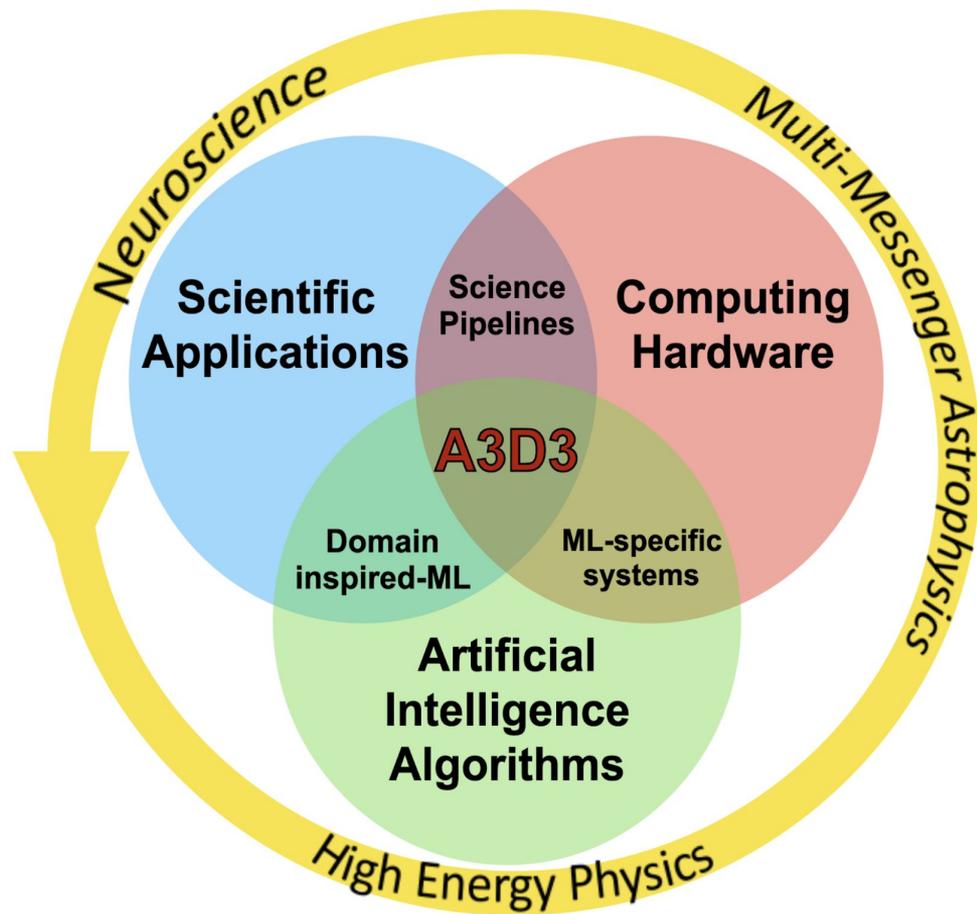
Accelerated AI
Algorithms for
Data-Driven
Discovery

NSF HDR Institute **A3D3** (since 2021)

Accelerated Artificial Intelligence Algorithms for Data-Driven Discovery

Our Mission is to enable **real-time AI techniques** for scientific and engineering discovery by uniting three core components: Scientific Applications, Artificial Intelligence Algorithms, and Computing Hardware.



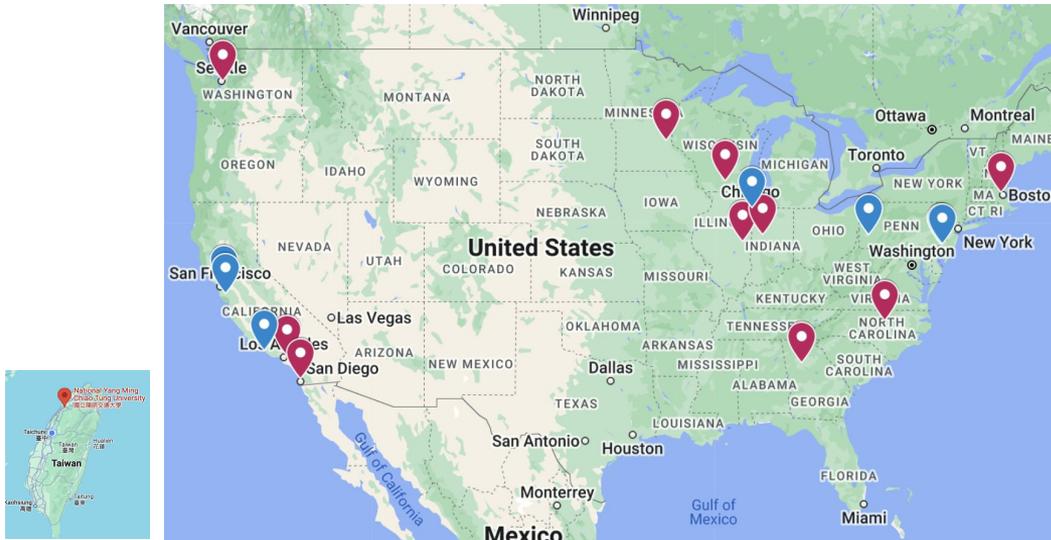


Multi-institution

NSF Harnessing the Data
Revolution Institute



21 institutions
170 members
(**75%** trainees)
(\$16M/5year)



Multi-disciplines

HEP

										
Hsu	Harris	Neubauer	Liu	Duarte	Rankin	Aarestad	Gonski	Carlsen	Cremonesi	Buat
PI/Director	co-PI	co-PI								

MMA

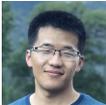
								
Coughlin	Scholberg	Graham	Riedel	Katsavounidis	Li	Sravan	DiPetrillo	Cavanaugh
co-PI	co-PI							

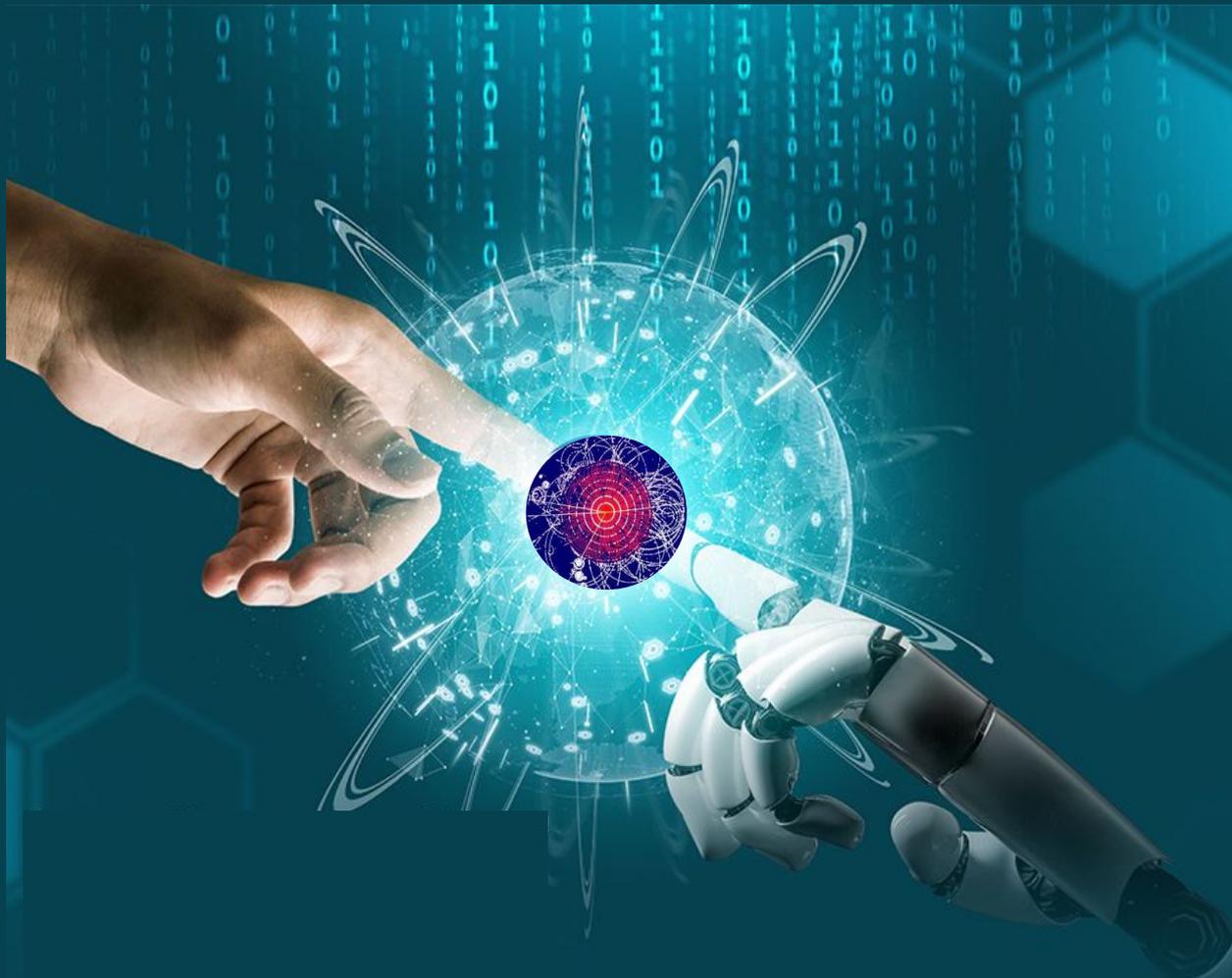
Neuros

				
Orsborn	Shlizerman	Dadarlat	Sun	Yu

35 faculty/staff

CS/EE

									
Hauck	Li	Chen	Han	Ju	Loncar	Liu	Li	Trivedi	Lai 賴伯承



Credit: Onpassive

Compute
Latency

1 ns

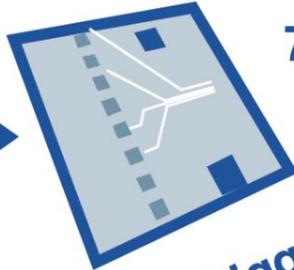
1 μ s

1 ms

1 s



40 MHz



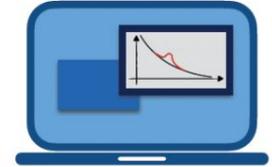
750 kHz

L1 Trigger



High-Level
Trigger

7.5 kHz
7 MB/evt



Offline

ASICs

FPGAs

CPUs

GPUs

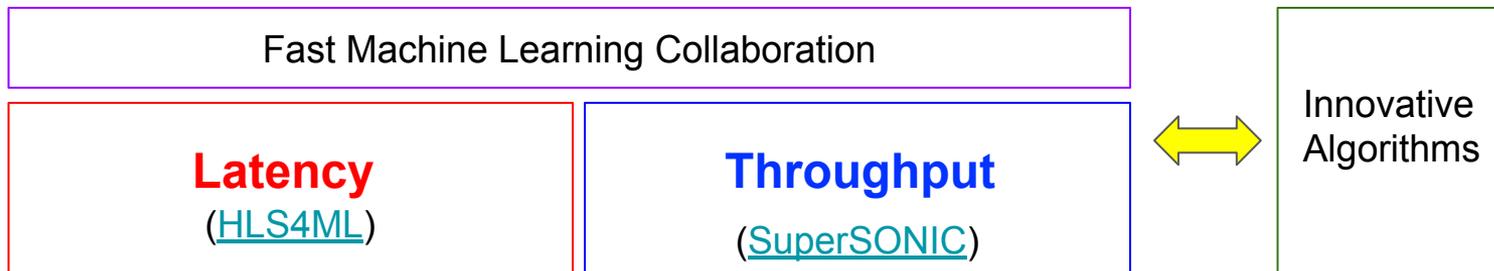
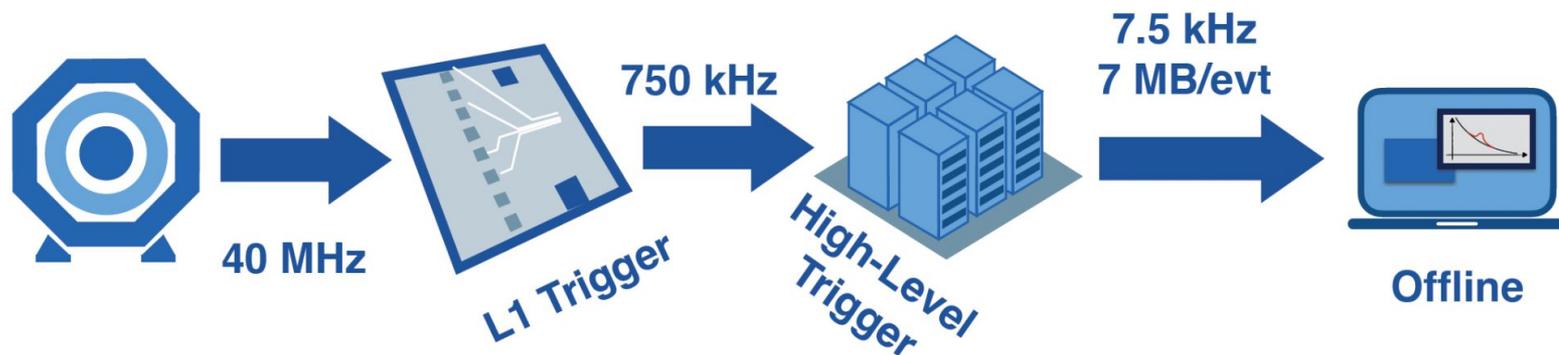
CPUs

GPUs

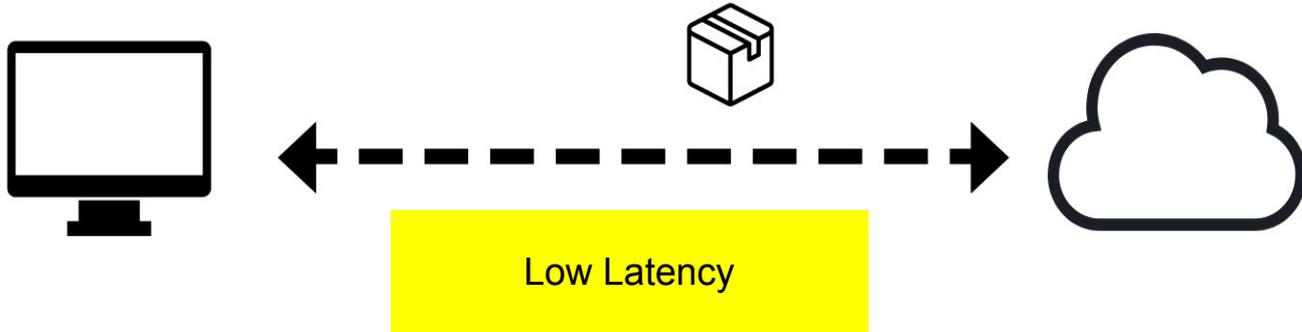
FPGAs

Exabyte-scale
datasets (10^{18} B)

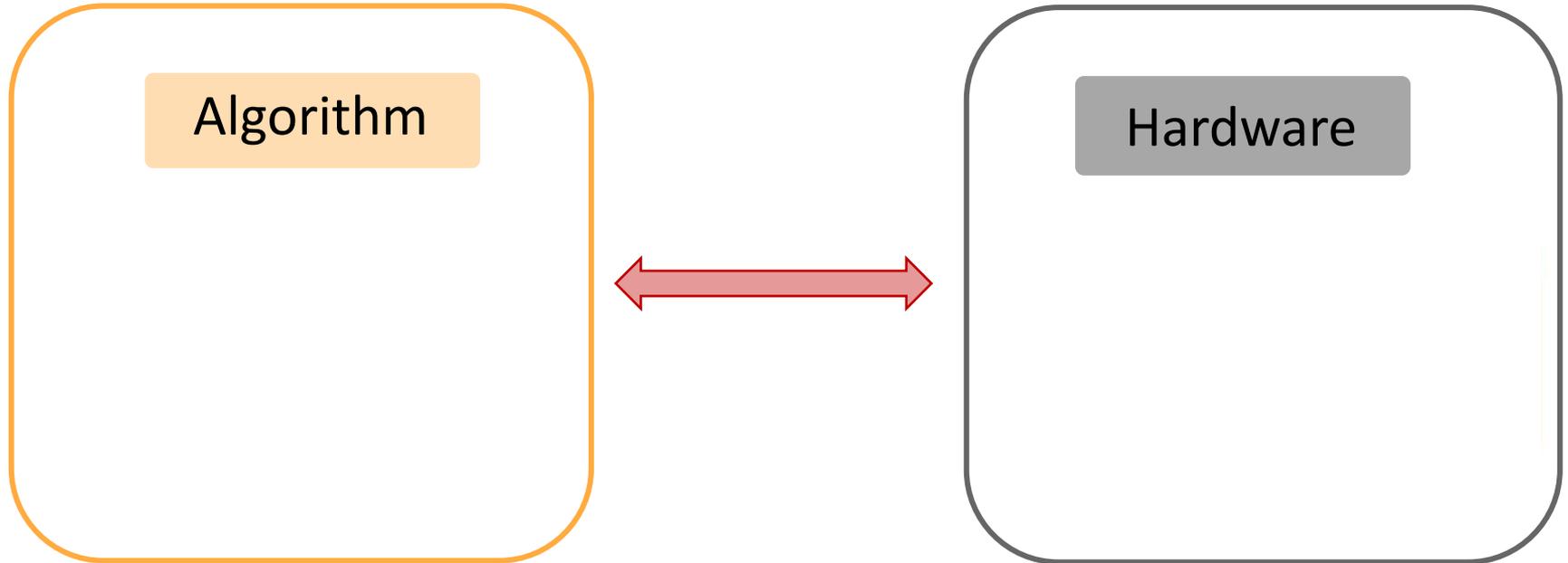
The Need for the FastML



Targeted system (FPGA/ASIC)



Hardware Algorithm Co-design, Automation



Hardware Algorithm Co-design, Automation

Algorithm

Tackle scientific data challenges:

- irregular data distributions
- scarce or limited labels
- interpretability and transparency of AI models.

Hardware

Hardware Algorithm Co-design, Automation

Algorithm

Tackle scientific data challenges:

- irregular data distributions
- scarce or limited labels
- interpretability and transparency of AI models.



Hardware

Dedicated platforms optimized to

- support these AI algorithms
- addressing the need for low latency, high throughput
- mindful consideration of power and memory constraints.

Hardware Algorithm Co-design, Automation



- Enable domain experts to implement and deploy AI algorithms directly on hardware.
- Streamline the conversion from algorithm development to hardware execution.



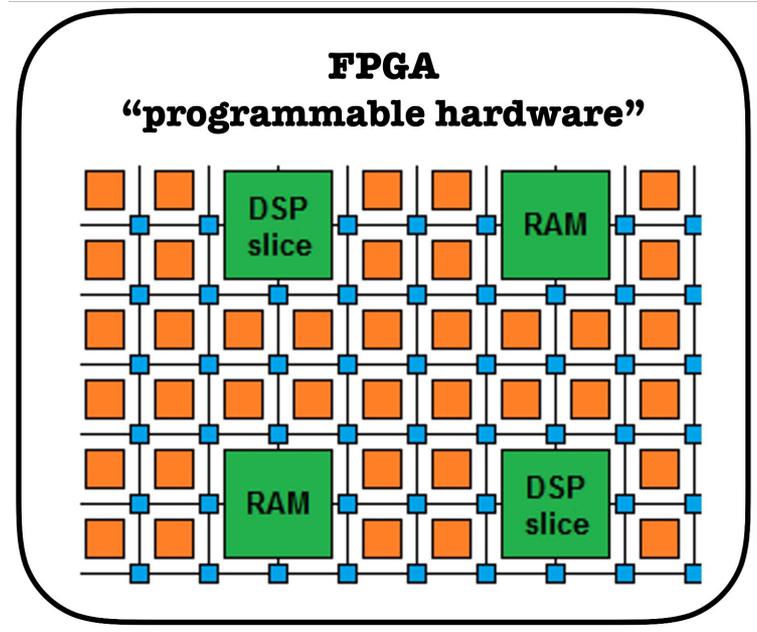
<https://github.com/fastmachinelearning/hls4ml>

▶ Pros:

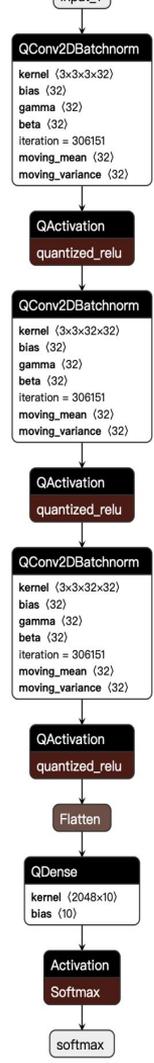
- ▶ Reprogrammable interconnects between embedded components that perform multiplication (DSPs), apply logical functions (LUTs), or store memory (BRAM)
- ▶ High throughput I/O: O(100) optical transceivers running at O(15) Gbps
- ▶ Massively parallel
- ▶ Low power

▶ Cons:

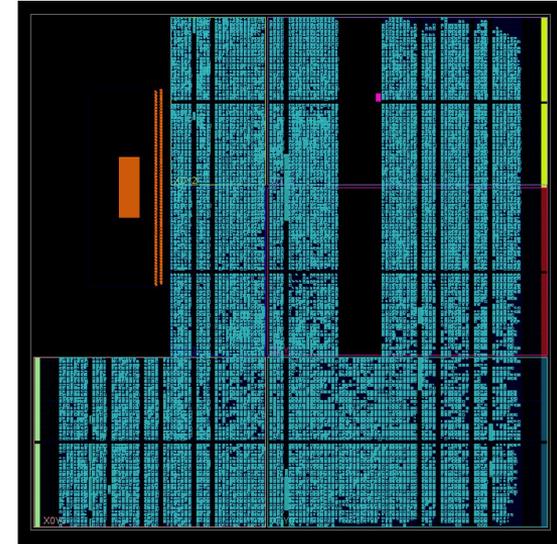
- ▶ Requires domain knowledge to program (using VHDL/Verilog)



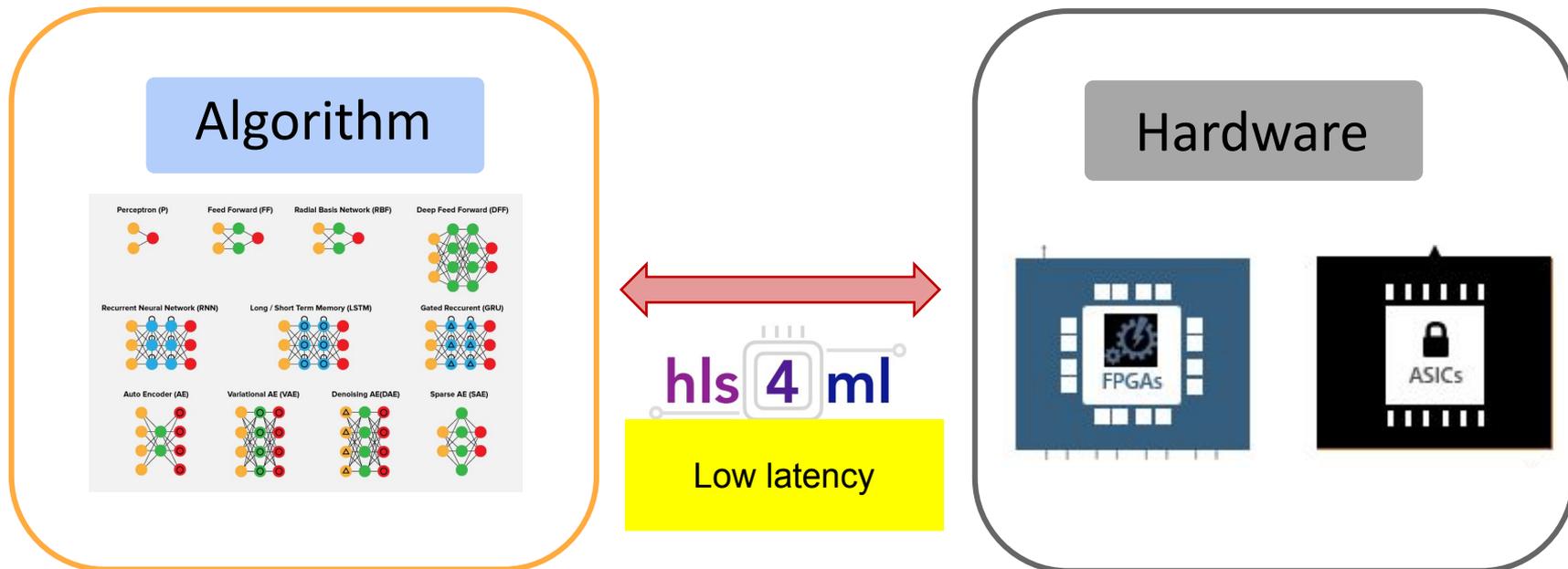
Programming Hardware (FPGAs)



High-Level Synthesis



Hardware Algorithm Co-design, Automation

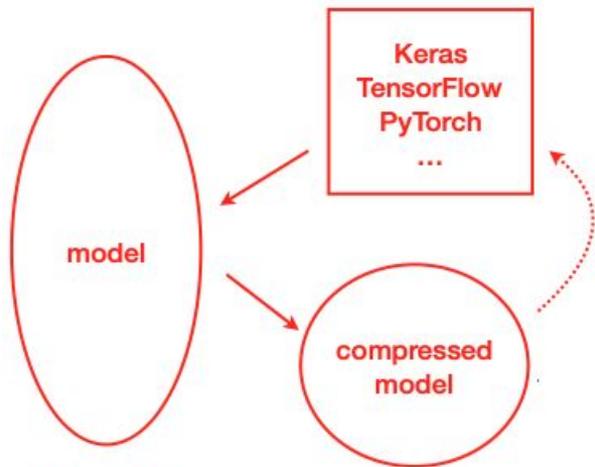


<https://github.com/fastmachinelearning/hls4ml>

HLS4ML translating ML into FPGA firmware



HLS4ML translating ML into FPGA firmware

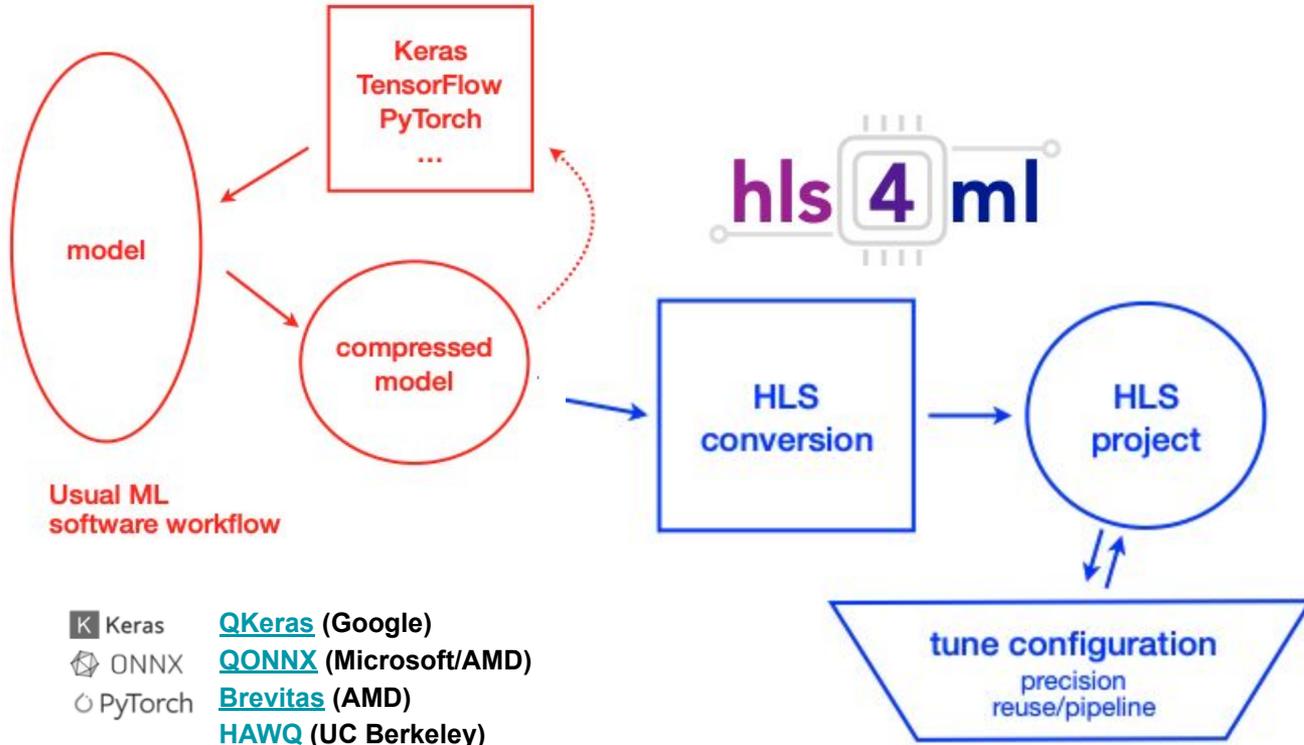


Usual ML software workflow

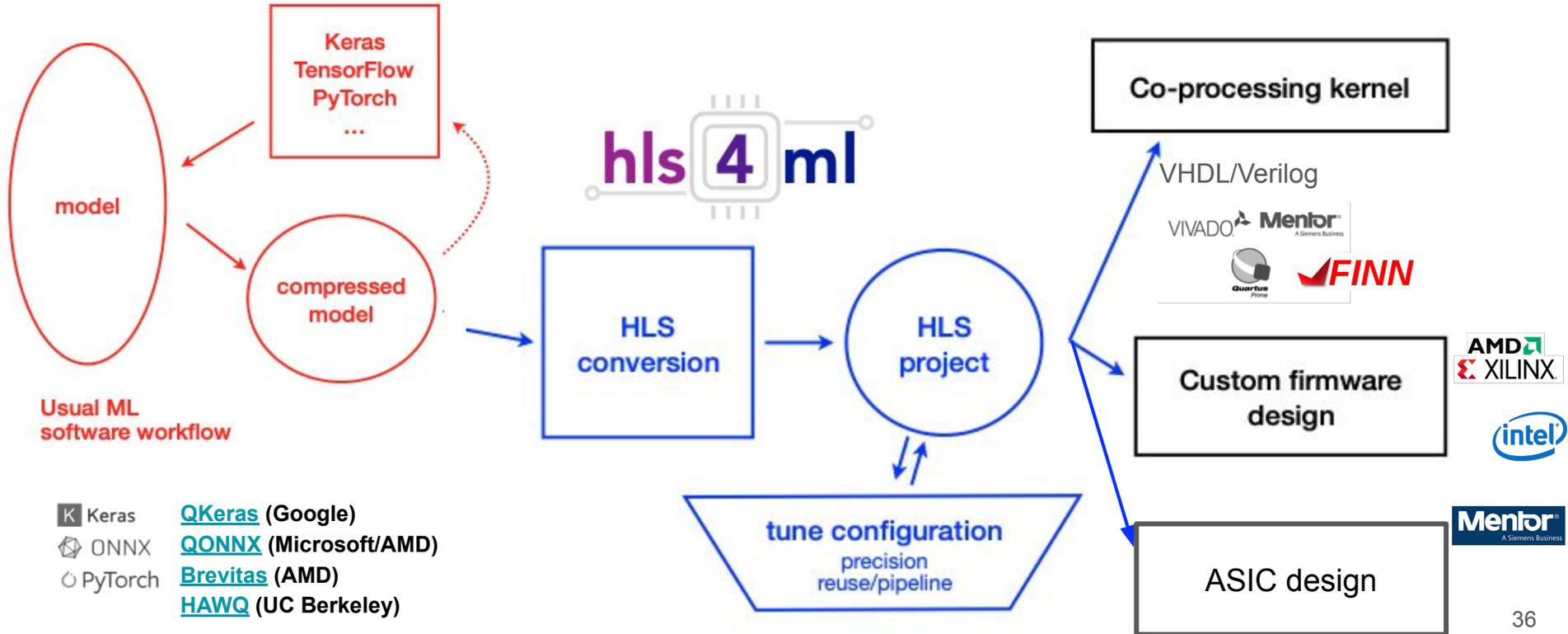


-  Keras [QKeras](#) (Google)
-  ONNX [QONNX](#) (Microsoft/AMD)
-  PyTorch [Brevitas](#) (AMD)
- [HAWQ](#) (UC Berkeley)

HLS4ML translating ML into FPGA firmware



HLS4ML translating ML into FPGA firmware

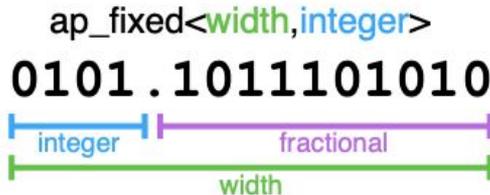


How can we accelerate an AI model on FPGA?

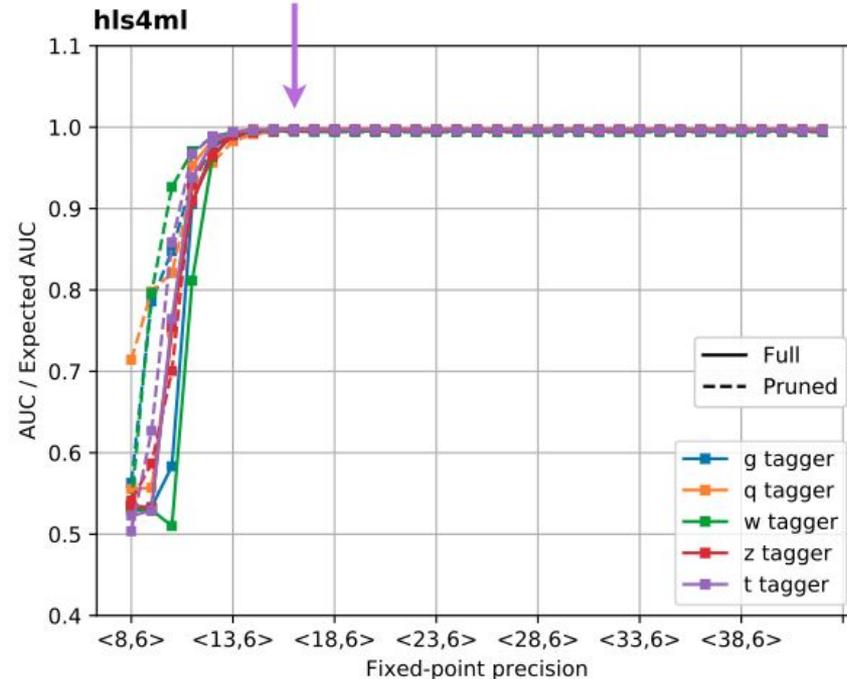
Quantization

Xilinx Vivado 2017.2
Clock frequency: 200 MHz
FPGA: Xilinx Kintex Ultrascale
(XCKU115-FLVB2104)

- ▶ Scan the bit width until you reach optimal performance

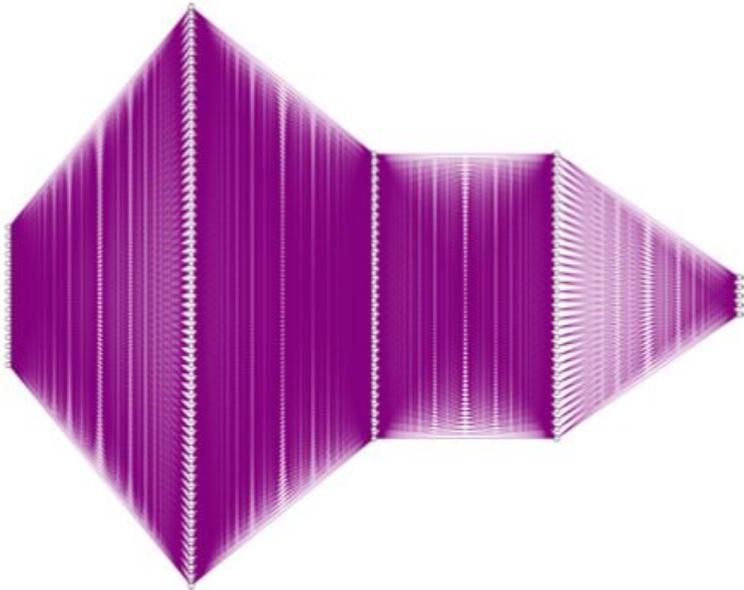


Full performance
with 16 bits



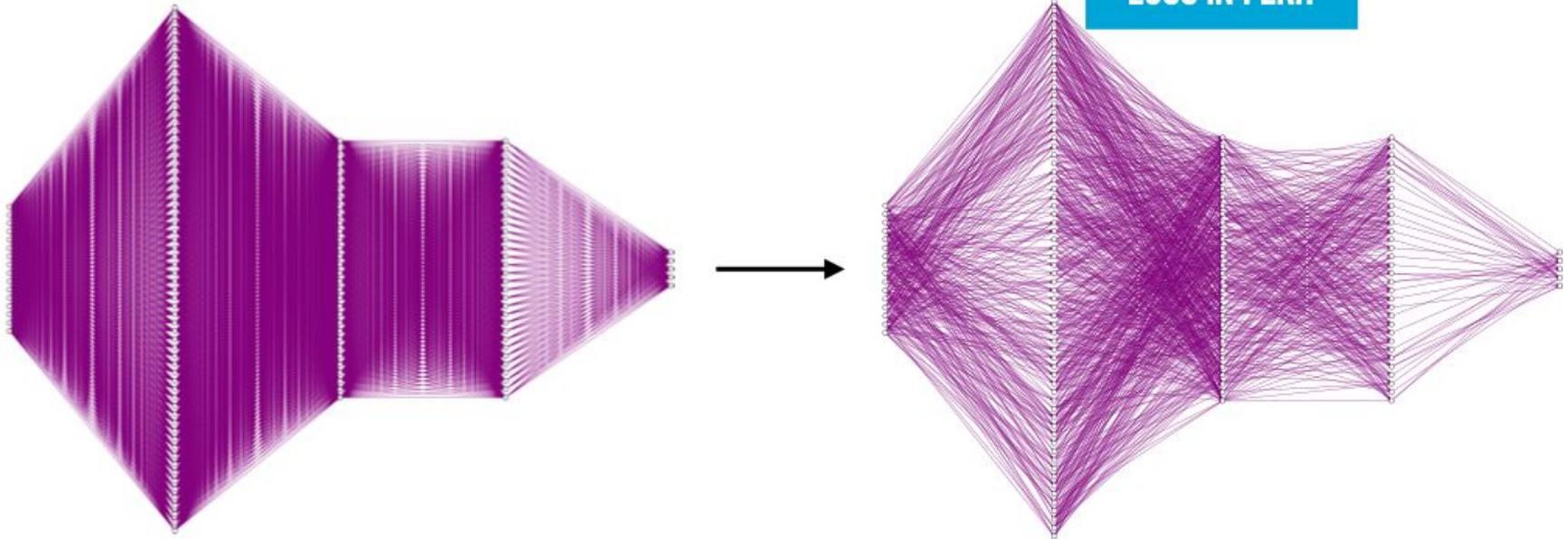
Pruning

- ▶ Remove **smallest** weight
- ▶ Iterate

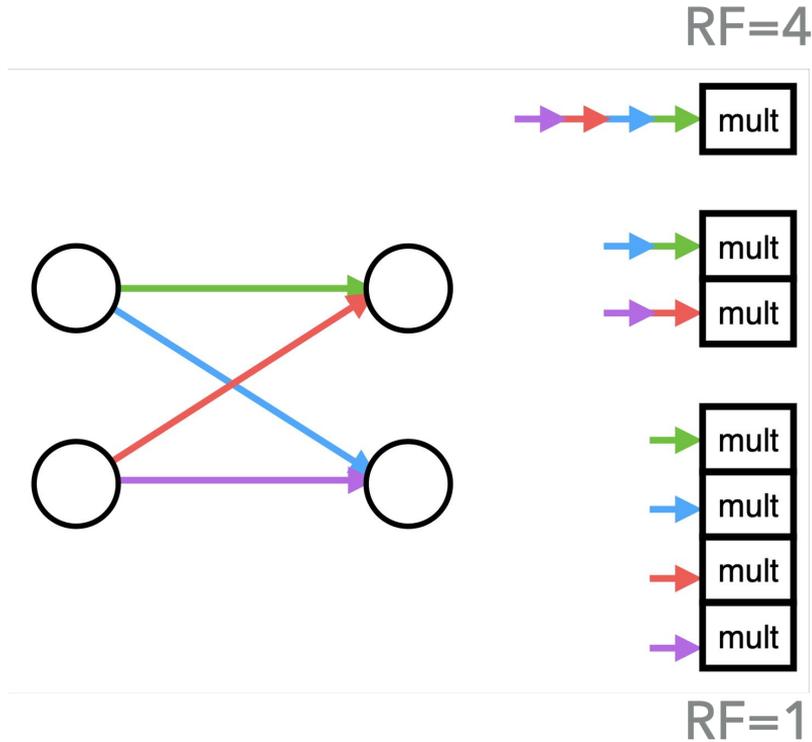


Pruning

- ▶ Remove **smallest** weights
- ▶ Iterate



Parallelization and Timing



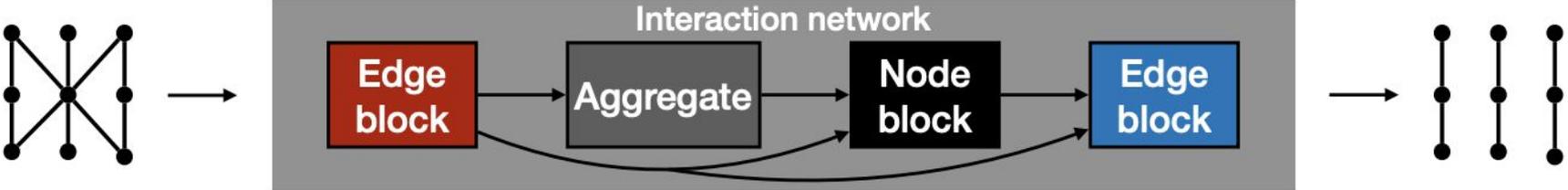
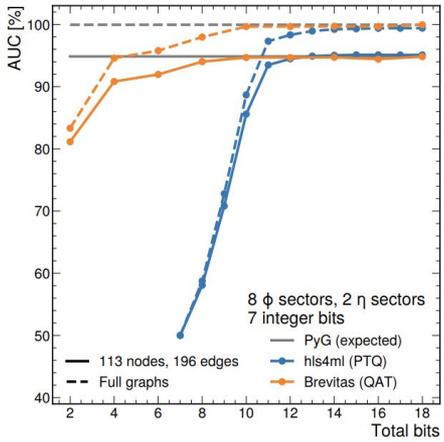
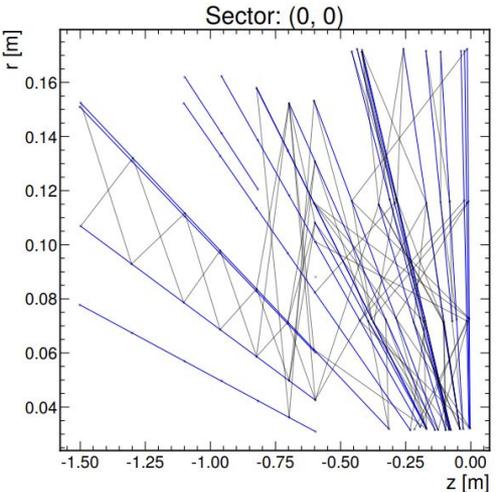
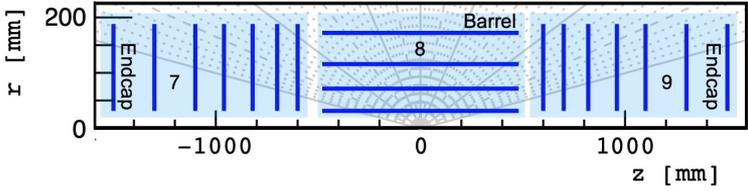
~35 clocks
@ 200 MHz
= 175 ns



~15 clocks
@ 200 MHz
= 75 ns

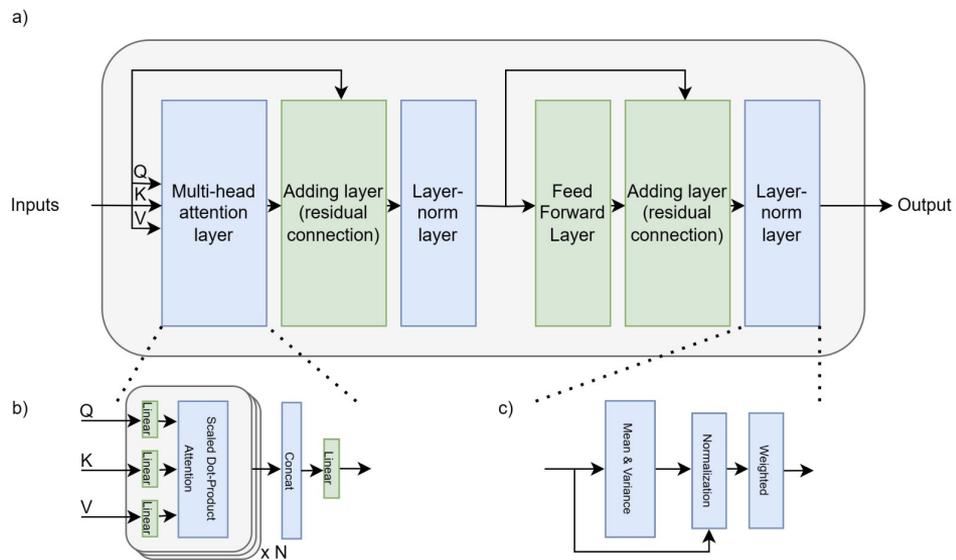
Graph Neural Networks for Tracking on FPGAs

[Front. Big Data, 23 March 2022](#)

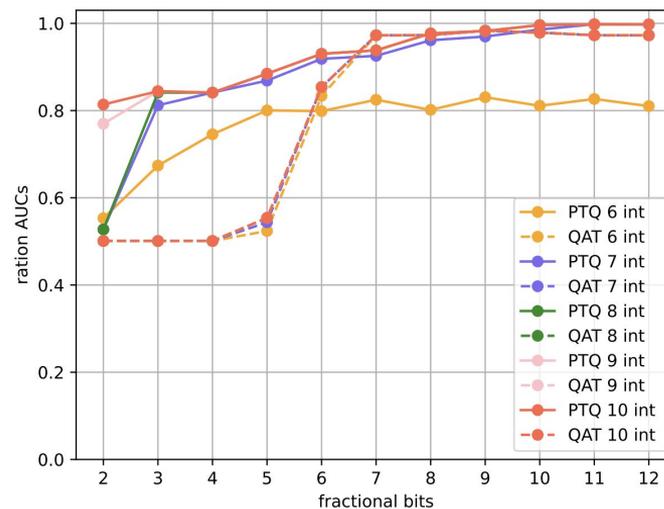


Transformer Inference on FPGAs

[Zhixing Jiang et al 2025 JINST 20 P04014](#)



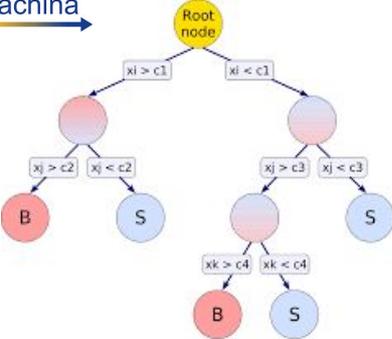
Flavor Tagging



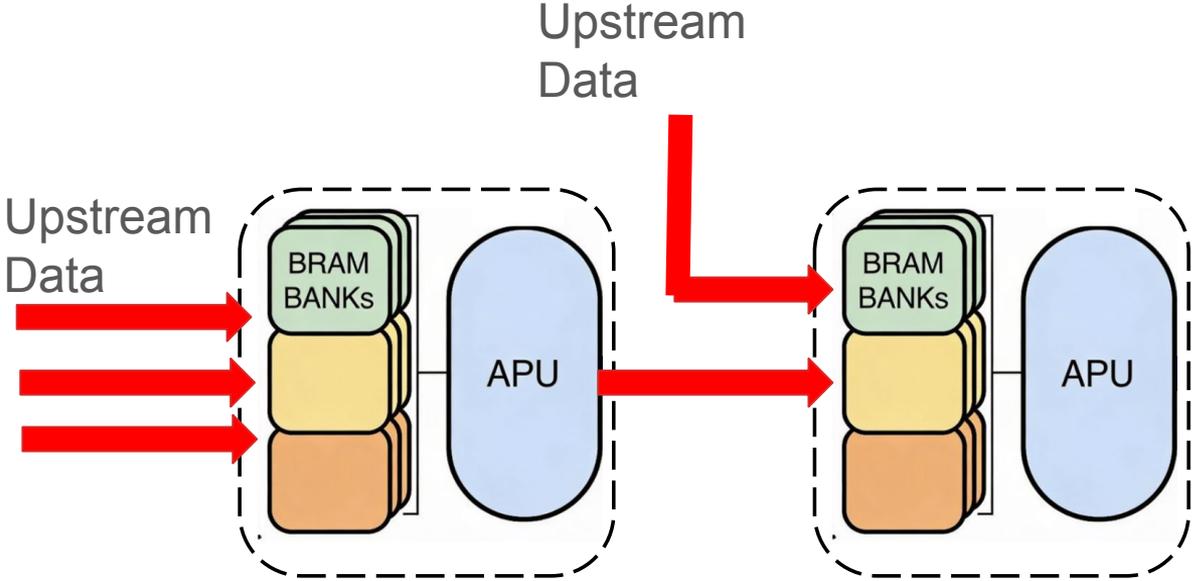
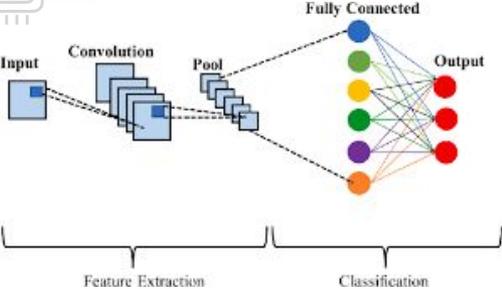
Global Event Processor Evaluation Platform

Zhixing Jiang et al 2024 JINST 19 P05031

FW X Machina

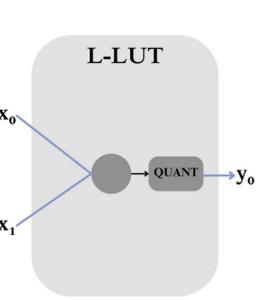


hls 4 ml



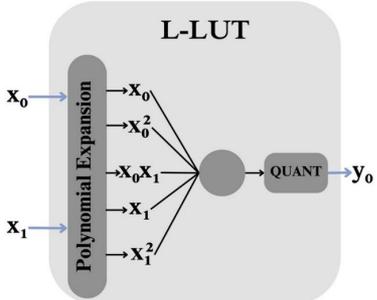
Evolution of LUT-based NNs

Andronic, Cassidy [FastML2025](#)



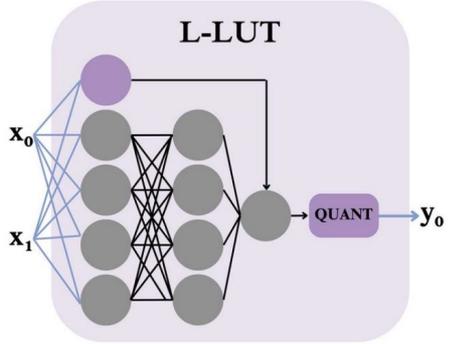
Neuron absorbed in a Logical LUT.

2020



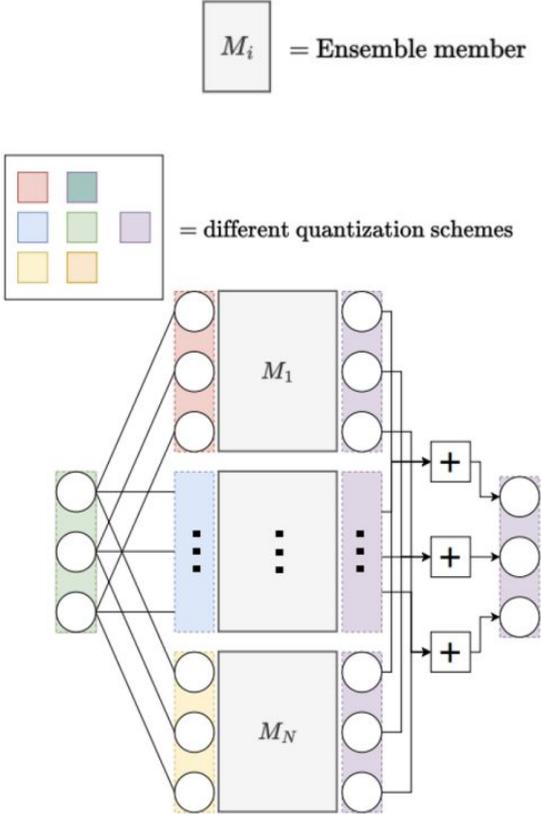
L-LUT hides a multivariate polynomial.

2023



Neuron hides MLP with skip connections.

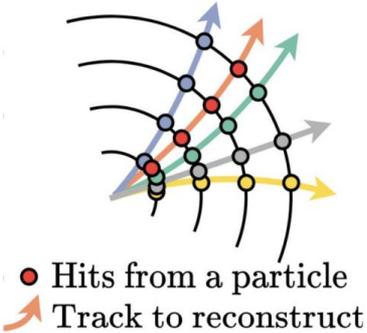
2024



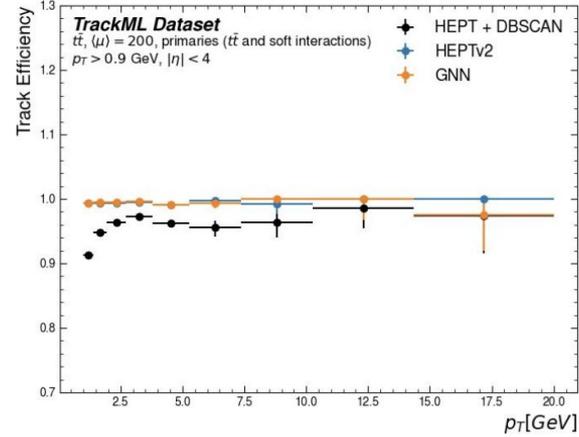
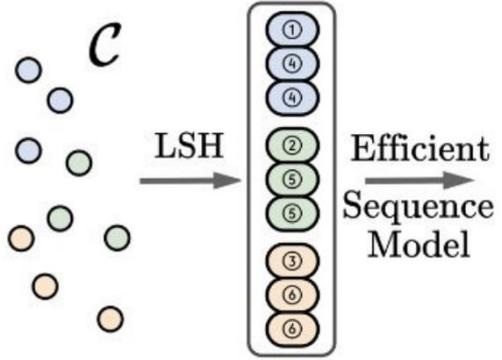
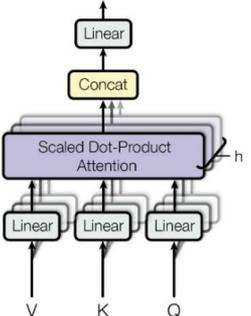
AmigoLUT

2025

Efficient Transformer Architectures for Point Cloud Data in High Energy Physics

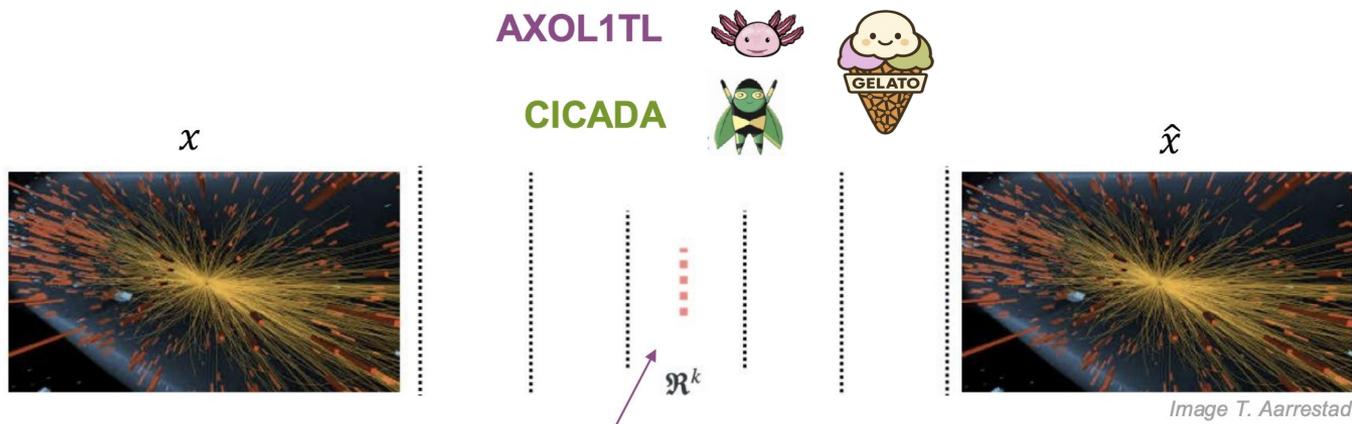


- Charged particles leave hits on multiple detector layers → point cloud, sparse, irregular
- Locality-Sensitive Hashing-Based Efficient Point Transformer (HEPT)



ANOMALY DETECTION AT 40 MHZ

- Anomaly detection algorithm for the trigger based on a variational autoencoder



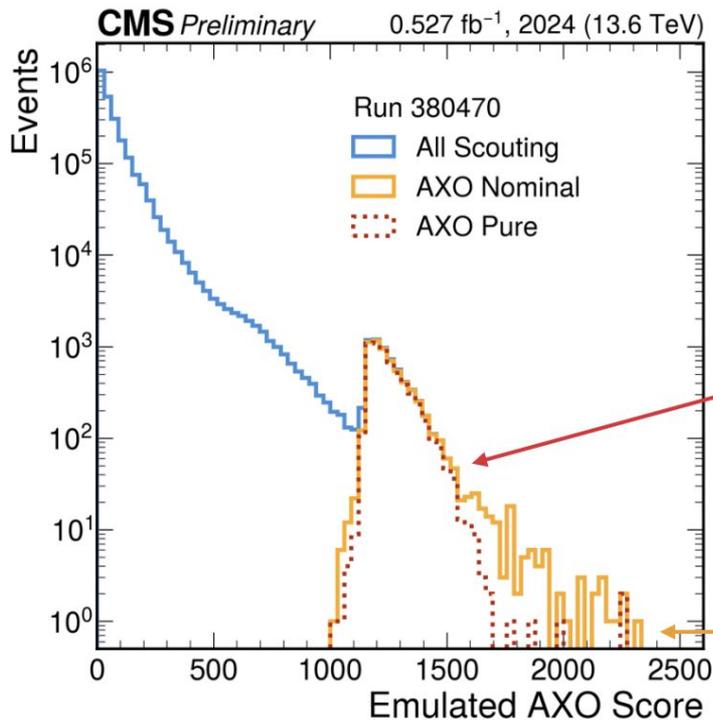
Train on randomly sampled *data*

Bottleneck: autoencoder learns to compress high dimensional inputs into low dimensional latent space

Unsupervised learning: $x - \hat{x}$ represents degree of abnormality

AXOL1TL triggered events

[CMS-DP-2024-059](#)

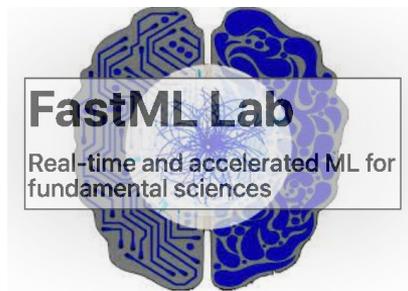


Large fraction of unique events recorded that would otherwise be rejected

High anomaly score events, also triggered by existing L1 trigger

Partnership and FastML Ecosystem

Growing strong industry connections with support through the [Fast ML community](#)



Partner Projects



Experiments



National & Int'l Laboratories



Coprocessors



IT Cloud Providers



High Performance Computing



A3D3 Postbac



Jada Marshall

Purdue University

Neuroscience

Supervisor: Maria Makin



Kira Nolan

CalTech

MMA

Supervisor: Matthew Graham



Lucie Afko

Duke University

HEP/MMA

Supervisor: Kate Scholberg



Malina Desai

MIT

MMA

Supervisors: Philip
Harris, Erik
Katsavounidis

Workshop & Conferences

- [Summer school](#)



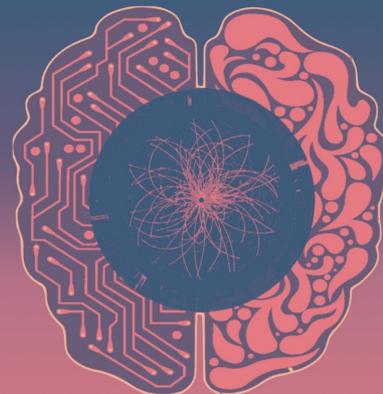
- [Workshop](#)



FAST MACHINE LEARNING FOR SCIENCE CONFERENCE

1-5 September 2025

ETH Zürich



Real-time and accelerated ML for fundamental sciences

Scientific Committee:

Thea K. Årrestad (ETH Zürich)
Javier Duarte (UCSD)
Phil Harris (MIT)
Burt Holzman (Fermilab)
Scott Hauck (U. Washington)
Shih-Chieh Hsu (U. Washington)
Sergo Jindariani (Fermilab)
Mia Liu (Purdue University)
Allison M. Deiana (Southern M. U.)

Mark Neubauer (U. Illinois U-C)
Jennifer Ngadiuba (Fermilab)
Maurizio Pierini (CERN)
Sioni Summers (CERN)
Alex Tapper (Imperial College)
Nhan Tran (Fermilab)

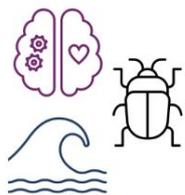
Organising Committee:

Thea K. Årrestad (ETH Zürich)
Marius Köppel (ETH Zürich)
Patrick Odagiu (ETH Zürich)
Anna Sfyrtla (UniGe)
Sioni Summers (CERN)
Jennifer Zollinger (ETH Zürich)

indi.to/fastml25



- [Conference](#)



Scientific-MOOD FAIR Challenge



2025 FPGA智慧運算與終端節點 創意應用競賽 暨 NSF HDR AI 黑客松競賽



FPGA競賽官網
<https://reurl.cc/eMvzAK>



NSF HDR AI黑客松官網
<https://indico.cern.ch/event/1610056/>



Summary

Real-time AI is transforming scientific and engineering discovery.

- **HLS4ML**: Speeds deployment of ML algorithms to FPGA/ASIC, optimizing workflows.
- **Expanding Ecosystem**: A growing community driving innovation across disciplines.





Shih-Chieh Hsu

<http://faculty.washington.edu/schsu/>
schsu@uw.edu

On-chip probabilistic inference for charged-particle tracking at the sensor edge

Arghya Ranjan Das et al [arXiv:2602.15946v2](https://arxiv.org/abs/2602.15946v2)

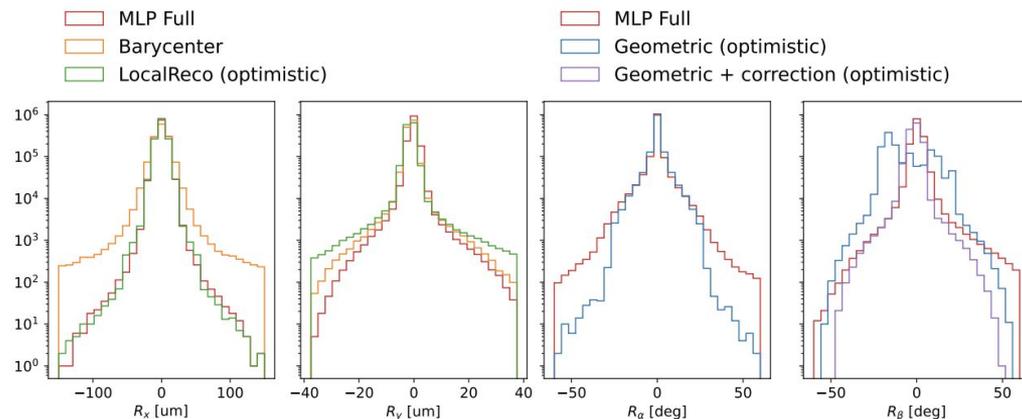
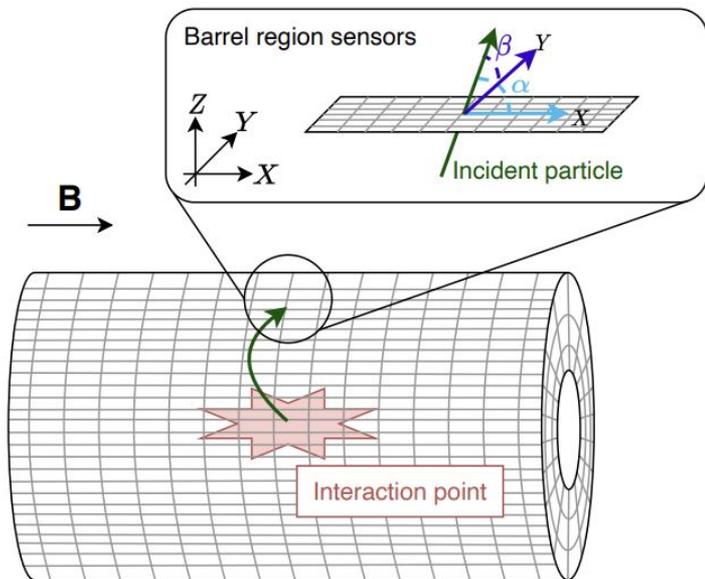
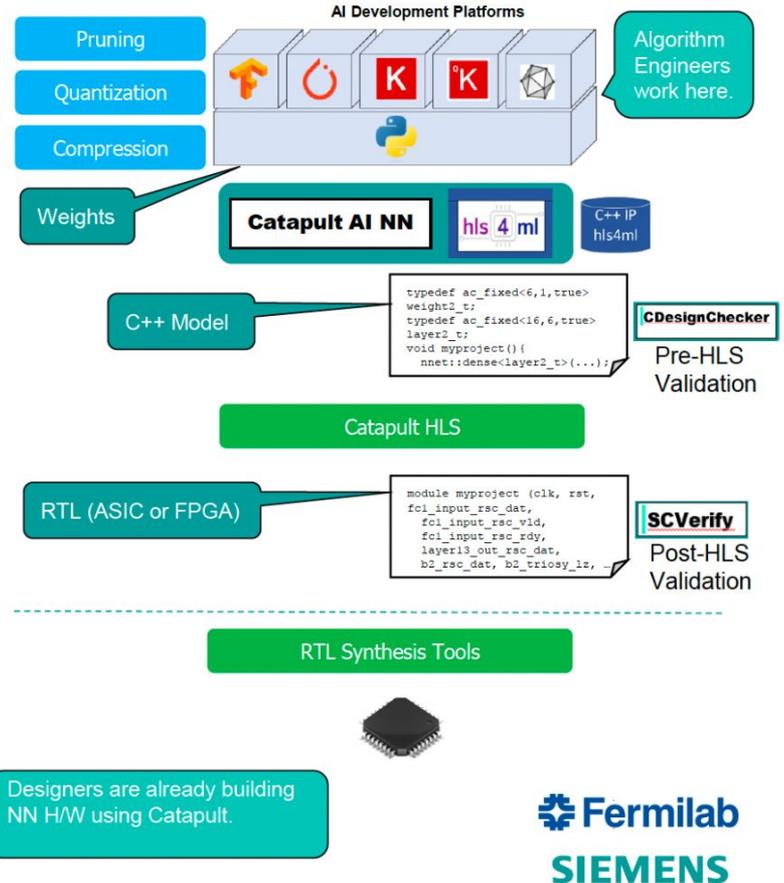


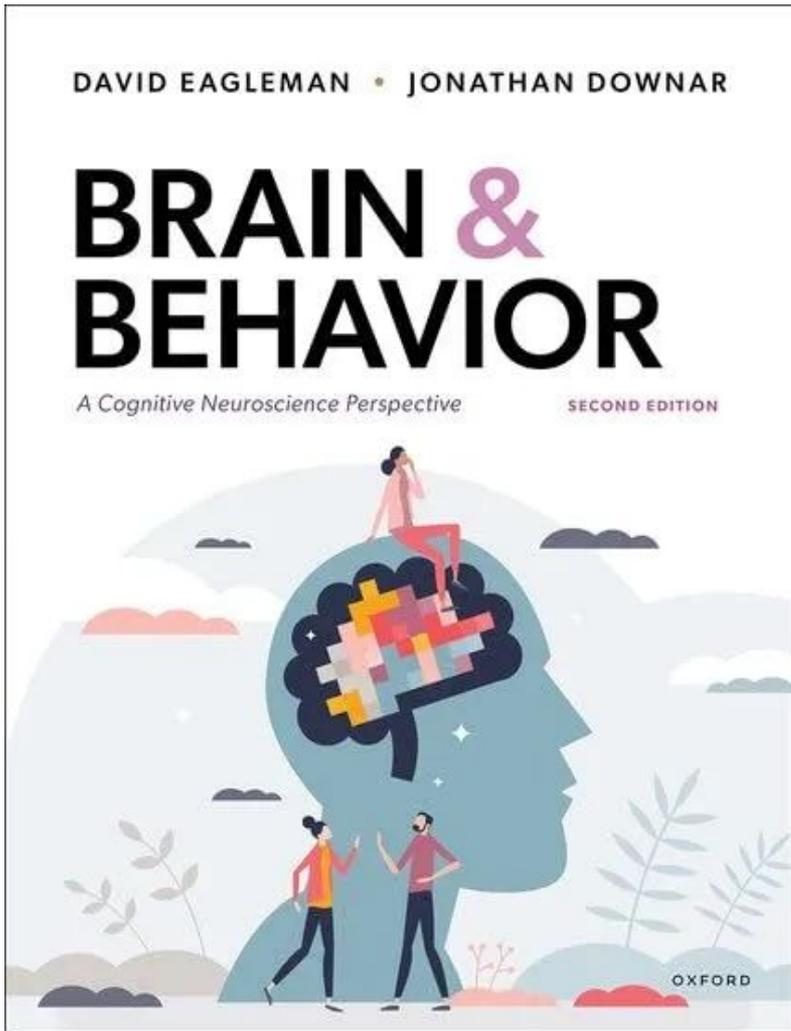
Figure 4: Comparison of the residuals for x , y , α , and β between the Full MLP model and non-ML algorithms. The non-ML algorithms labeled as “optimistic” incorporate information that is not directly available on the ASIC.

What is HLS4ML?

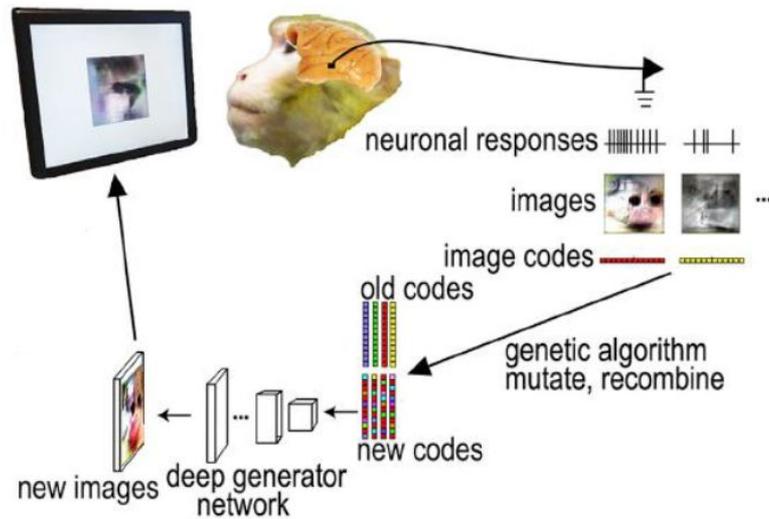
- A Python package that:
 - Generates a top-level C++ design leveraging a library of C++ machine learning (ML) functions
 - The generated C++ code is a dataflow pipeline of hardened layers
 - Compiles the synthesis-ready C++ design into register-transfer level (RTL) code using High-level synthesis (HLS) tools (FPGA or ASIC)
 - Provides coarse-grained “reuse_factor” for latency/resource control to explore hardware implementations
 - Provides fully parallel or streamed input/output

Catapult allows designers to target ASIC platforms

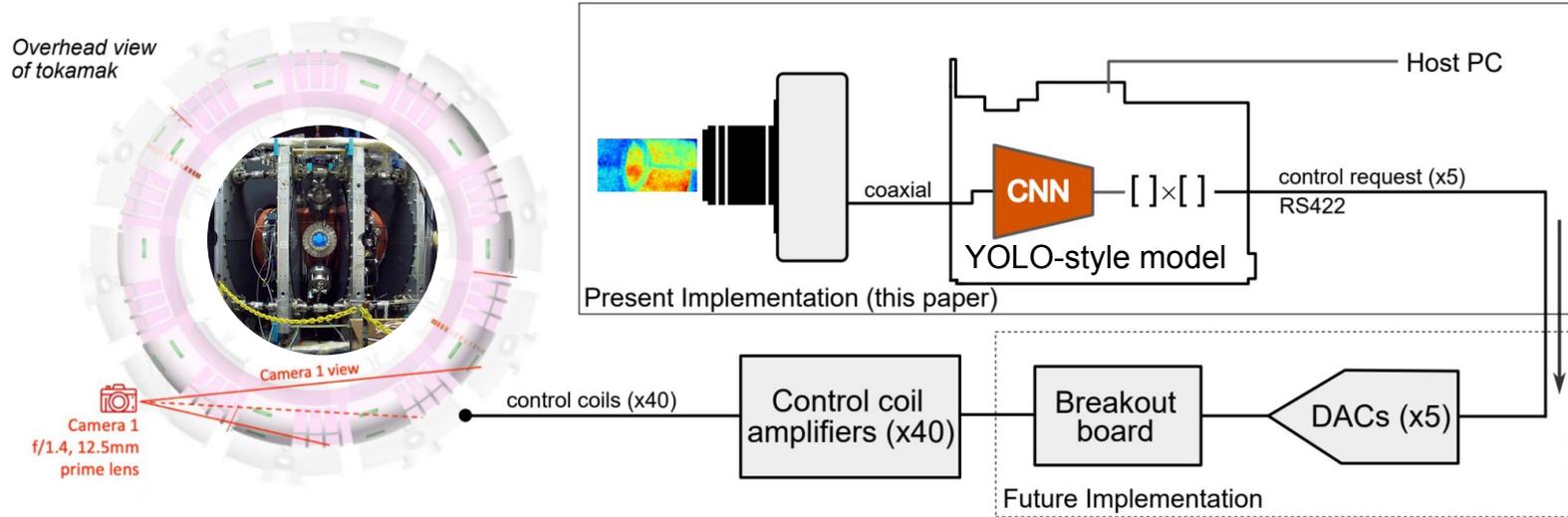




Change stimuli based on brain activity →
map responses quickly



Fusion: in-situ inference on frame grabber FPGAs in high-speed imaging

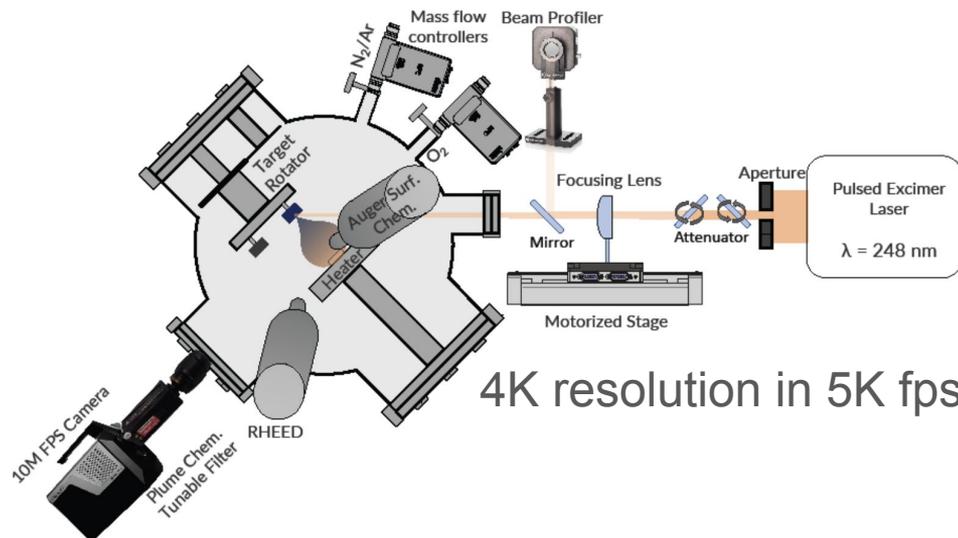
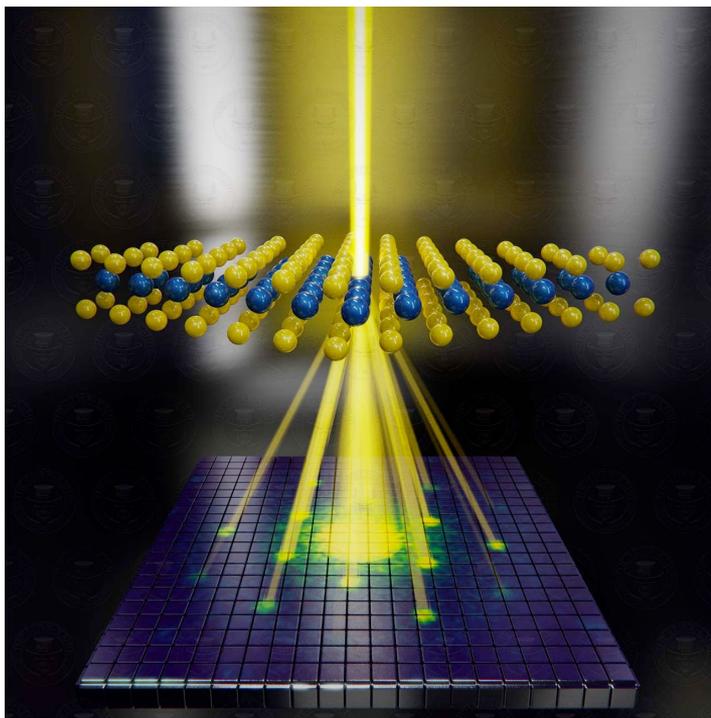


Fusion magneto hydrodynamics and
crystal structure detection

[Rev. Sci. Instrum. 95, 073509 \(2024\)](#)

4D Scanning Transmission Electron Microscopy

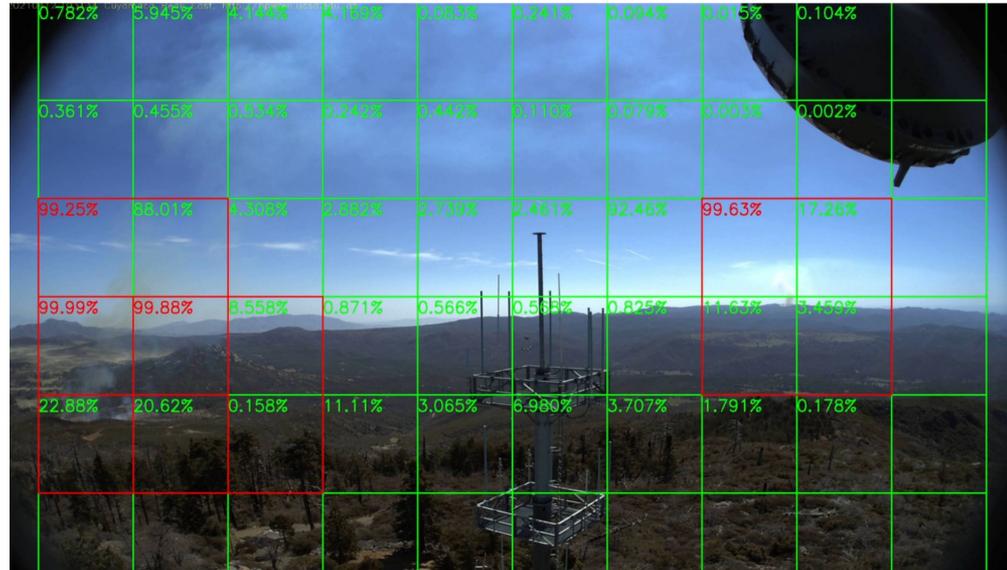
[Agar FastML talk](#)



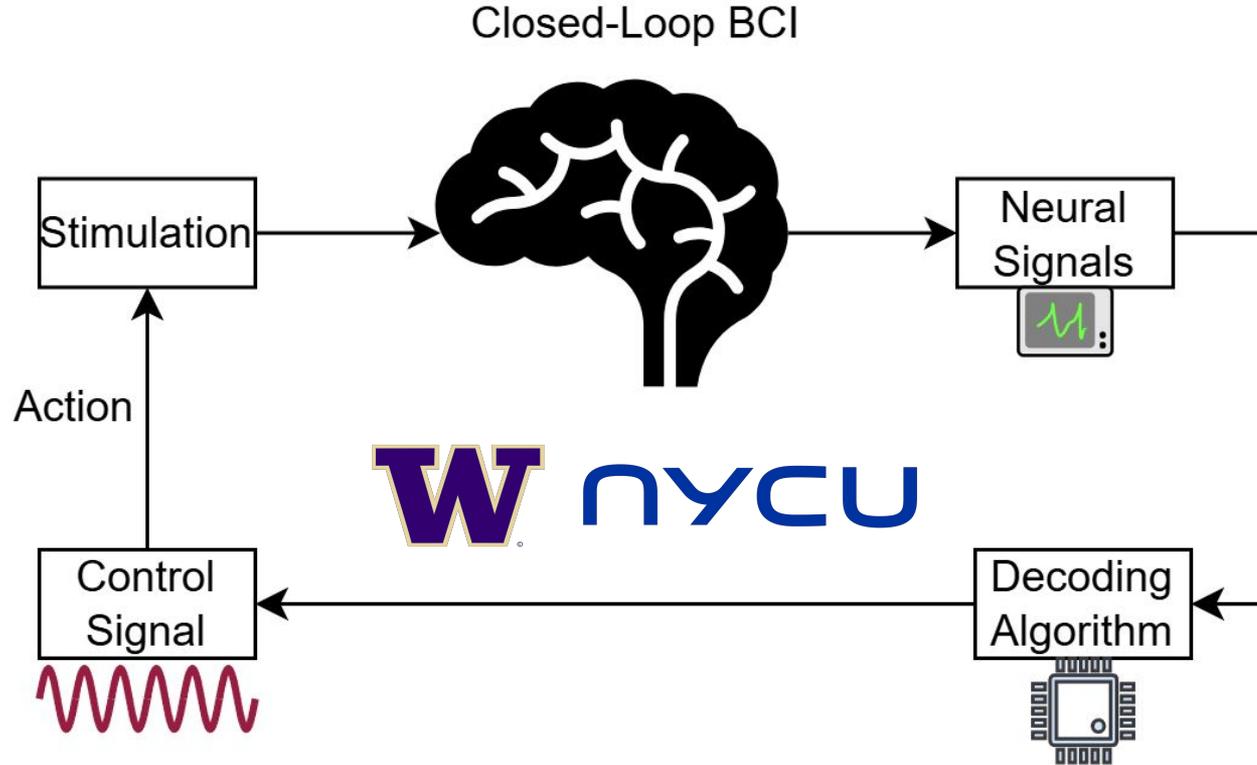
4K resolution in 5K fps

Wildfire: Enabling Embedded Systems and IoT

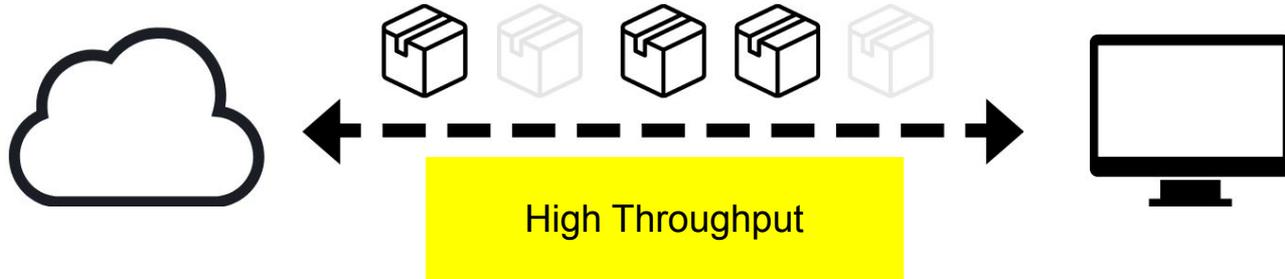
Utilization of hls4ml to integrate AI detection models (trained with PyTorch and TensorFlow-Keras) onto FPGAs, demonstrating the effectiveness of this approach for rapid and efficient wildfire detection and prevention strategies.



Closed-Loop Brain Stimulation

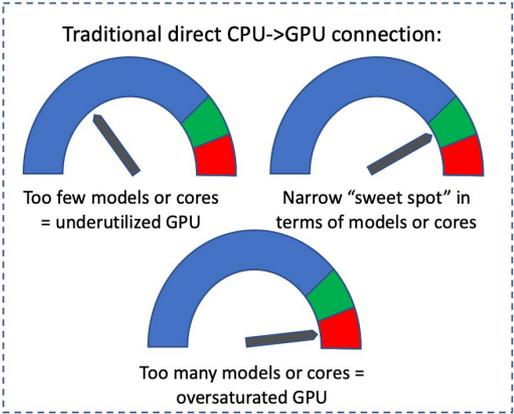
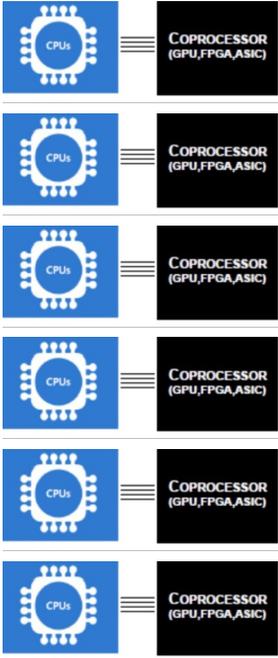


Heterogeneous System

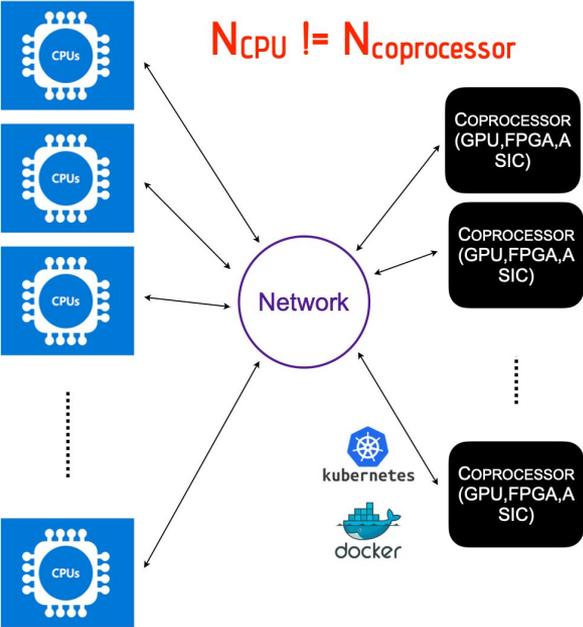


Coprocessor Integration Approaches

1. Direct connection
Inflexible, expensive



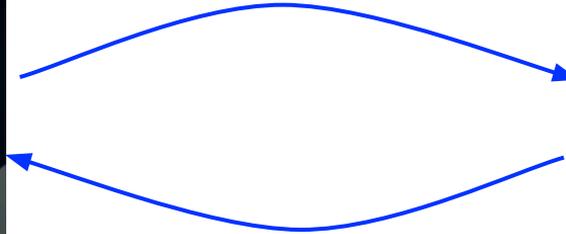
2. "As a service"
Complex, requires R&D



Not so different from ChatGPT!



What to do in Kaohsiung in
Summer 2025?



Let's go dragon boat racing!

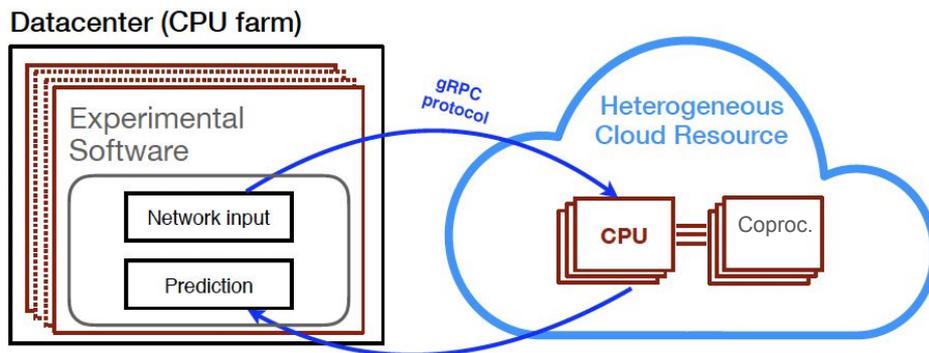


A computing paradigm adaptive to changing hardware landscape

Services for **O**ptimized **N**etwork **I**nfERENCE on **C**o-processors.

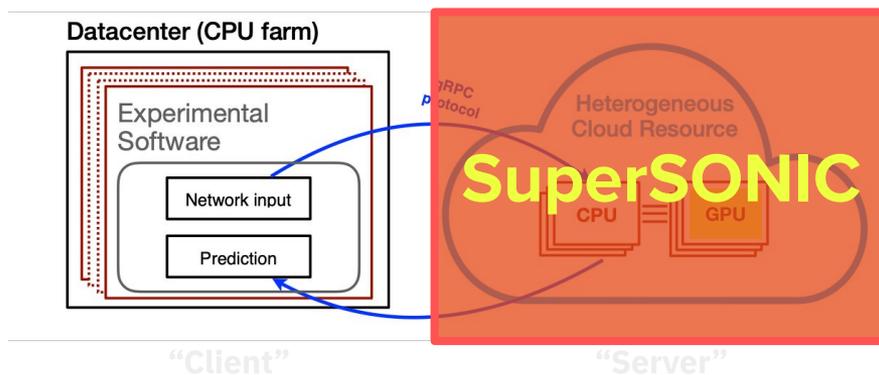
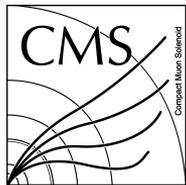
“Inference-as-a-Service”:

- Client–server architecture
- Data sent to GPU/FPGA server via gRPC
- Results returned synchronously or asynchronously



SuperSONIC

- SuperSONIC implements SONIC server infrastructure as a portable package based on open-source industry-standard tools.
- GitHub: <https://github.com/fastmachinelearning/SuperSONIC>



Client workflows vary between experiments, but server feature needs are largely similar.

Many applications can benefit from a common server implementation.

Gravitational Wave Data workflow for Alerts

Multi-messenger Astrophysics

Rapidly identify all signals from multi-messenger events

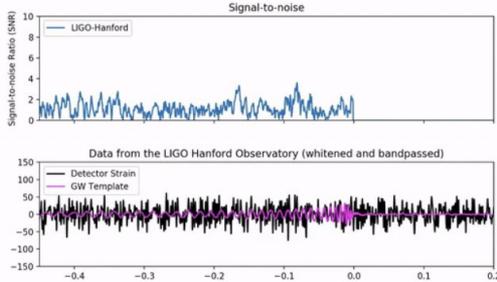
DETECTOR CHARACTERISATION



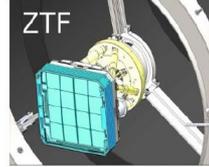
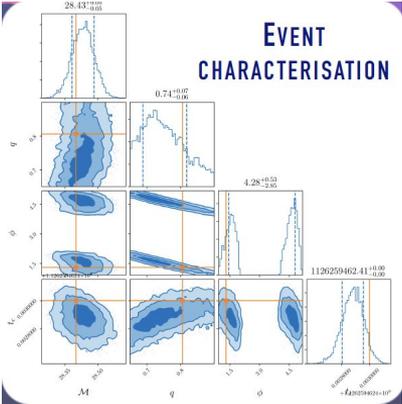
USE INFO FROM WITNESS SENSORS TO PERFORM DATA DE-NOISING



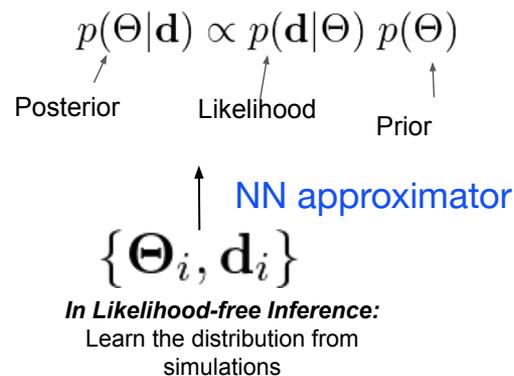
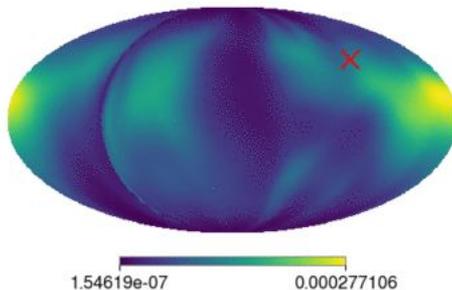
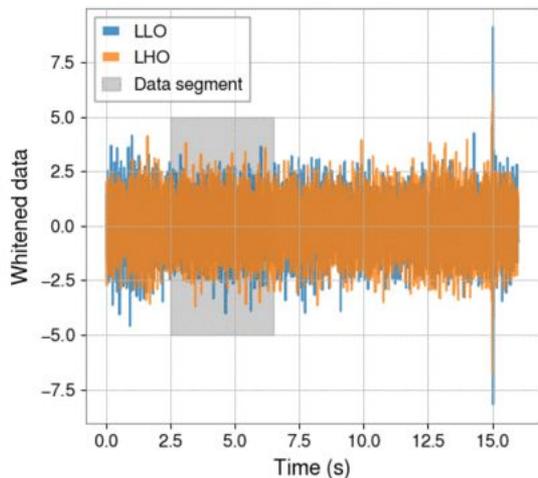
EVENT DETECTION



EVENT CHARACTERISATION



MMA: Aframe + AMPLFI deployed Summer 2025!



MMA: Aframe + AMPLFI deployed Summer 2025!

GCN Circular 41606

Subject LIGO/Virgo/KAGRA S250830bp: Identification of a GW compact binary merger candidate
Event [LIGO/Virgo/KAGRA S250830bp](#)
Date 2025-08-30T10:55:06Z (4 days ago)
From Pedro Jeronimo Santos da Silva <pedro.jeronimo@unesp.br>
Via Web form

The LIGO Scientific Collaboration, the Virgo Collaboration, and the KAGRA Collaboration report:

We identified the compact binary merger candidate S250830bp during real-time processing of data from LIGO Hanford Observatory (H1), LIGO Livingston Observatory (L1), and Virgo Observatory (V1) at 2025-08-30 10:24:18.852 UTC (GPS time: 1440584676.852). The candidate was found by the Aframe [1], cWB [2], cWB BBH [3], GstLAL [4], MBTA [5], Mly [6], PyCBC Live [7], and SPIIR [8] analysis pipelines.

S250830bp is an event of interest because its false alarm rate, as estimated by the online analysis, is $3.2e-10$ Hz, or about one in $1e2$ years. The event's properties can be found at this URL:

Two sky maps are available at this time and can be retrieved from the GraceDB event page:

* `amplfi.multiorder.fits.0`, an initial localization generated by AMPLFI [10], distributed via GCN and SciMMA notices about 24 seconds after the candidate event time.

* `bayestar.multiorder.fits.0`, an initial localization generated by BAYESTAR [11], distributed via GCN and SciMMA notices about 5 minutes after the candidate event time.

The preferred sky map at this time is `bayestar.multiorder.fits.0`. For the `bayestar.multiorder.fits.0` sky map, the 90% credible region is 11 deg^2 . Marginalized over the whole sky, the a posteriori luminosity distance estimate is $429 \pm 100 \text{ Mpc}$ (a posteriori mean \pm standard deviation).

- Made the first Compact Binary Coalescence discovery using NNs
 - [S250904cv](#), [S250904br](#), [S250904ae](#), [S250904af](#), [S250904ag](#), [S250904ah](#), [S250904ai](#), [S250904aj](#), [S250904ak](#), [S250904al](#), [S250904am](#), [S250904an](#), [S250904ao](#), [S250904ap](#), [S250904aq](#), [S250904ar](#), [S250904as](#), [S250904at](#), [S250904au](#), [S250904av](#), [S250904aw](#), [S250904ax](#), [S250904ay](#), [S250904az](#), [S250904ba](#), [S250904bb](#), [S250904bc](#), [S250904bd](#), [S250904be](#), [S250904bf](#), [S250904bg](#), [S250904bh](#), [S250904bi](#), [S250904bj](#), [S250904bk](#), [S250904bl](#), [S250904bm](#), [S250904bn](#), [S250904bo](#), [S250904bp](#), [S250904bq](#), [S250904br](#), [S250904bs](#), [S250904bt](#), [S250904bu](#), [S250904bv](#), [S250904bw](#), [S250904bx](#), [S250904by](#), [S250904bz](#), [S250904ca](#), [S250904cb](#), [S250904cc](#), [S250904cd](#), [S250904ce](#), [S250904cf](#), [S250904cg](#), [S250904ch](#), [S250904ci](#), [S250904cj](#), [S250904ck](#), [S250904cl](#), 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