2 Design

2.1 CONTROL VME Registers

2.1.1 Register Table

VME register map of CONTROL FPGA.

address	register name	R/W	initial value	size
0	CONTROL_RESET	R/W	0	1
1	CONTROL_I2C	R/W	0000	4
2	CONTROL_DEBUG	R/W	0	1

2.1.2 CONTROL_RESET (address 0)

Reset to RX and TX FPGAs. Logical add of CONTROL_RESET and external reset works as Global reset which resets all RX and TX FPGAs.

CONTROL FPGA itself is reset by external reset only. External reset is a push-button reset on the board, VME SYSRST or J3 TTCRST.

Note: J3 TTCRST is made not to work now. (J3 TTCRST doesn't connect with the external reset line in FPGA.)

bit	0
reg	RST
R/W	R/W
initial value	0

- RST

  Positive logic. 1=reset. 0=remove reset.

2.1.3 CONTROL_I2C (1)

I^2C for TTCrx on SPP.

bit	3	2	1	0
reg	SCL_R	SCL_W	SDA_R	SDA_W
R/W	R	R/W	R	R/W
initial value	0	0	0	0

2.1.4 CONTROL_DEBUG (2)

An instruction to start test patterns to all RX_FPGAs at once.

Start=1. Test patterns stop when TP_FIFO in RX_FPGA becomes empty.

bit	0
reg	GBL_TPSTART
R/W	R/W
initial value	0

2.2 RX VME Registers

2.2.1 Register Table

The VME register map of RX_FPGA is shown and explained below.

Registers other than RX_CHANNEL_TO_SLEEP_ are implemented using a voting logic structure.

When undefined addresses (from 22 to 31) are read, the value 0xabcd will be returned. (0xabcd is 1010_1011_1100_1101 as a binary number.)

address	register name	R/W	initial value	size
Initial setting				
0	RX_INITIAL_SETTING	R/W	1111_0111_0111_0111	16
JTAG				
1	RX_JRC_JTAG_1	R/W	0000_0000_0000_0011	16
2	RX_SLB_JTAG_1	R/W	0000_0000_0000_0011	16
3	RX_JRC_JTAG_2	R/W	0000_0000_0000_0011	16
4	RX_SLB_JTAG_2	R/W	0000_0000_0000_0011	16
LVDS link				
5	RX_SSW_SEND_SYNC_1	R/W	0000_0000_0000_0000	16
6	RX_SSW_SEND_SYNC_2	R/W	0000_0000_0000_0000	16
Error check of PDAs				
7	RX_PDA_ERRORS	R	0001_0001_0001_0001	16
Checks of FIFO state				
8	RX_OVERFLOW_0	R	0000_0000	8
9	RX_OVERFLOW_1	R	0000_0000	8
10	RX_OVERFLOW_2	R	0000_0000	8
11	RX_OVERFLOW_3	R	0000_0000	8
12	RX_FIFO_STATUS	R/W	0_0000_1111	9
Reset to each RX				
13	RX_RST	R/W	0000	4
SLEEP (Not be implemented now)				
14	RX_CHANNEL_TO_SLEEP_	R/W	1111	4
Test patterns				
15	RX_TP_WRITE	R/W	0100_0000_0000_0000	16
16	RX_TP_SETTING	R/W	0100_0000_0000_0000	16
Dumps				
17	RX_DMP_SETTING	R/W	0100_0000_0000_0000	16
18	RX_DMP_READ_0	R	0100_0000_0000_0000	16

19	RX_DMP_READ_1	R	0100_0000_0000_0000	16
20	RX_DMP_READ_2	R	0100_0000_0000_0000	16
21	RX_DMP_READ_3	R	0100_0000_0000_0000	16

2.2.2 RX_INITIAL_SETTING (0)

RX initial setting. It is enough to be set only when an experiment begins.

bit	15	14	13	12	11	10	9	8
reg	EDGE_CS	NEED_NXT3	NEED_CUR3	NEED_PRV3		NEED_NXT2	NEED_CUR2	NEED_PRV2
R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W
initial value	1	1	1	1	0	1	1	1

bit	7	6	5	4	3	2	1	0
reg		NEED_NXT1	NEED_CUR1	NEED_PRV1		NEED_NXT0	NEED_CUR0	NEED_PRV0
R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W
initial value	0	1	1	1	0	1	1	1

- NEED_NXT/CUR/PRV0/1/2/3

  Selects data lines to be read among NXT, CUR and RPV lines from SLB0/1/2/3.
  Read=1. Not read=0.

- EDGE_CS

  Selects between the positive edge or the negative edge with which cs_ (chip select signal from TX) is taken. This selection is valid for all edges of 4 RX in 1 FPGA at once.
  posedge=1. negedge=0.

2.2.3 RX_JRC_JTAG_1 (1)

A JTAG register for controlling JRC on PS board_1.

PS board_1 is shown in Figure 23.

Not only JTAG setting but also LVDS link's state are read out, and whether JTAG information are delivered correctly or not is checked.

bit	15	14	13	12	11	10	9	8
reg			PSLINK_ BAD_NOW1	PSLINK_ BAD_ONCE1	SSWLINKA_ BAD_NOW1	SSWLINKA_ BAD_ONCE1	SSWLINKB_ BAD_NOW1	SSWLINKB_ BAD_ONCE1
R/W	R	R	R	R	R	R	R	R
initial value	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
reg					JRC_TDO1	JRC_TCK1	JRC_TMS1	JRC_TDI1
R/W	R	R	R	R	R	R/W	R/W	R/W
initial value	0	0	0	0	0	0	1	1

- JRC_TDO1, JRC_TCK1, JRC_TMS1, JRC_TDI1

  A JTAG register for controlling JRC on PS board_1.

- PSLINK_BAD_NOW

  Shows link state of a LVDS deserializer (PSLINK) of PS board_1. Locked=0. Unlocked=1.

- PSLINK_BAD_ONCE

  Indicates whether PSLINK has unlocked or not. Locked always=0. Unlocked once=1.
  This register value is reset to be zero when the FPGA receives reset signal or when RX_JRC_JTAG_1, RX_SLB_JTAG_1 or RX_SSW_SERI_RST registers are read.

- SSWLINKA/B_BAD_NOW

  Shows link state of LVDS deserializer (SSWLINKA/B_) of SSW.
  Locked=0. Unlocked=1.

- SSWLINKA/B_BAD_ONCE

  Indicates whether SSWLINKA/B_ has unlocked or not. Locked always=0. Unlocked once=1.
  This register value is reset to be zero when the FPGA receives reset signal or when RX_JRC_JTAG_1, RX_SLB_JTAG_1 or RX_SSW_SERI_RST registers are read.

2.2.4 RX_SLB_JTAG_1 (2)

A JTAG register for controlling SLB ASICs or PP ASICs on PS board_1.

Not only JTAG setting but also LVDS link's state are read out, and whether JTAG information are delivered correctly or not is checked.

bit	15	14	13	12	11	10	9	8
reg			PSLINK_ BAD_NOW1	PSLINK_ BAD_ONCE1	SSWLINKA_ BAD_NOW1	SSWLINKA_ BAD_ONCE1	SSWLINKB_ BAD_NOW1	SSWLINKB_ BAD_ONCE1
R/W	R	R	R	R	R	R	R	R
initial value	0	0	0	0	0	0	0	0
bit	7	6	5	4	3	2	1	0
reg					SLB_TDO1	SLB_TCK1	SLB_TMS1	SLB_TDI1
R/W	R	R	R	R	R	R/W	R/W	R/W
initial value	0	0	0	0	0	0	1	1

- SLB_TDO1, SLB_TCK1, SLB_TMS1, SLB_TDI1

  A JTAG register for controlling Slave Board ASICs or Patch Panel ASICs on PS board_1.

2.2.5 RX_JRC_JTAG_2 (3)

A JTAG register for controlling JRC on PS board_2.

PS board_2 is shown in Figure 23. In FPGA5 and FPGA6, PS board_2 doesn't exist and RX_JRC_JTAG_2 does nothing.

Not only JTAG setting but also LVDS link's state are read out, and whether JTAG information are delivered correctly or not is checked.

bit	15	14	13	12	11	10	9	8
reg			PSLINK_ BAD_NOW2	PSLINK_ BAD_ONCE2	SSWLINKA_ BAD_NOW2	SSWLINKA_ BAD_ONCE2	SSWLINKB_ BAD_NOW2	SSWLINKB_ BAD_ONCE2
R/W	R	R	R	R	R	R	R	R
initial value	0	0	0	0	0	0	0	0
bit	7	6	5	4	3	2	1	0
reg					JRC_TDO2	JRC_TCK2	JRC_TMS2	JRC_TDI2
R/W	R	R	R	R	R	R/W	R/W	R/W
initial value	0	0	0	0	0	0	1	1

2.2.6 RX_SLB_JTAG_2 (4)

A JTAG register for controlling SLB ASICs or PP ASICs on PS board_2.

In FPGA5 and FPGA6 (Figure 23), PS board_2 doesn't exist and RX_SLB_JTAG_2 does nothing.

Not only JTAG setting but also LVDS link's state are read out, and whether JTAG information are delivered correctly or not is checked.

bit	15	14	13	12	11	10	9	8
reg			PSLINK_ BAD_NOW2	PSLINK_ BAD_ONCE2	SSWLINKA_ BAD_NOW2	SSWLINKA_ BAD_ONCE2	SSWLINKB_ BAD_NOW2	SSWLINKB_ BAD_ONCE2
R/W	R	R	R	R	R	R	R	R
initial value	0	0	0	0	0	0	0	0
bit	7	6	5	4	3	2	1	0
reg					SLB_TDO2	SLB_TCK2	SLB_TMS2	SLB_TDI2
R/W	R	R	R	R	R	R/W	R/W	R/W
initial value	0	0	0	0	0	0	1	1

2.2.7 RX_SEND_SYNC_1 (5)

A command to force LVDS serializers concerning PS Board_1 to output SYNC patterns. These LVDS serializers are located on both a SSW module and PS board_1. (Figure 22)

bit	15	14	13	12	11	10	9	8
reg			PSLINK_ BAD_NOW1	PSLINK_ BAD_ONCE1	SSWLINKA_ BAD_NOW1	SSWLINKA_ BAD_ONCE1	SSWLINKB_ BAD_NOW1	SSWLINKB_ BAD_ONCE1
R/W	R	R	R	R	R	R	R	R
initial value	0	0	0	0	0	0	0	0
bit	7	6	5	4	3	2	1	0
reg						PSSYNC_T1	PSSYNC_R1	SSWSYNC1
R/W	R	R	R	R	R	R/W	R/W	R/W
initial value	0	0	0	0	0	0	0	0

- SSWSYNC

SYNC command for LVDS serializer on a SSW module. Set SYNC mode=1. Normally=0.

- PSSYNC_T

  SYNC command for LVDS serializers which send SLB trigger output on PS Board_1. Set SYNC mode=1. Normally=0.

- PSSYNC_R

  SYNC command for LVDS serializers which send SLB readout output on PS Board_1. Set SYNC mode=1. Normally=0.

2.2.8 RX_SEND_SYNC_2 (6)

A command to force LVDS serializers concerning PS Board_2 to output SYNC patterns. These LVDS serializers are located on both a SSW module and PS board_2.

bit	15	14	13	12	11	10	9	8
reg			PSLINK_ BAD_NOW2	PSLINK_ BAD_ONCE2	SSWLINKA_ BAD_NOW2	SSWLINKA_ BAD_ONCE2	SSWLINKB_ BAD_NOW2	SSWLINKB_ BAD_ONCE2
R/W	R	R	R	R	R	R	R	R
initial value	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
reg						PSSYNC_T2	PSSYNC_R2	SSWSYNC2
R/W	R	R	R	R	R	R/W	R/W	R/W
initial value	0	0	0	0	0	0	0	0

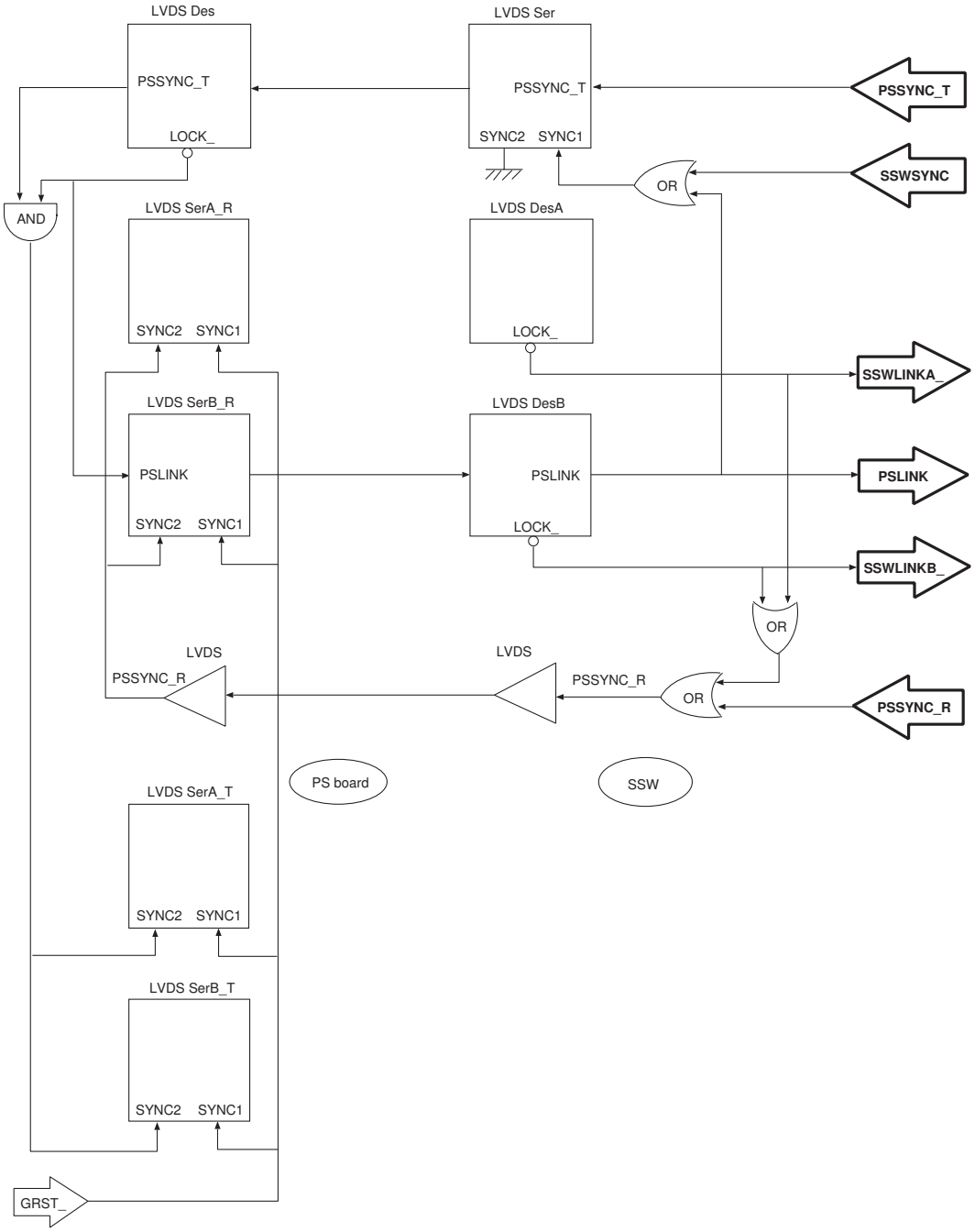

Figure 22: Locations of PSLINK, SSWLINKA/B, SSWSYNC and PSSYNC_R/T signals

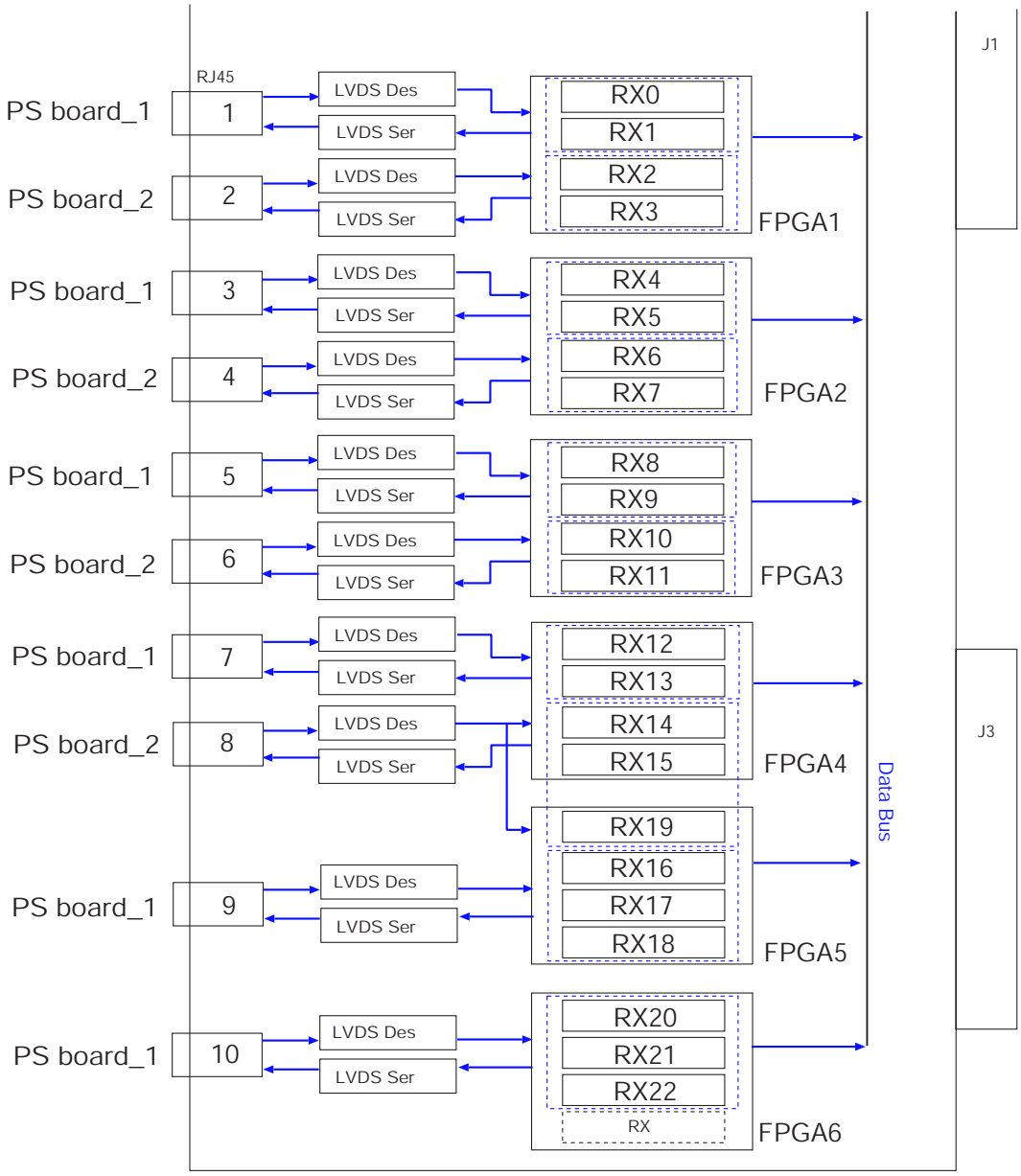

Figure 23: Assignment of PS board_1 or PS board_2. FPGA5 and FPGA6 don't have PS board_2.

2.2.9 RX_PDA_ERRORS (7)

Registers which tell errors in Phase_Difference_Absorber (PDA).

PDA is a sub-block in RX FPGA, which absorbs difference between wclk and rclk. Wclk is the clock signal from a LVDS deserializer. Rclk is the clock signal of a data-bus. (FPGAs work in synchronization with rclk.)

PDA receives data in synchronization with wclk, and sends data in synchronization with rclk.

bit	15	14	13	12	11	10	9	8
reg		PDA_ ERR3	PDA_ FULL_SYNC3	PDA_ EMPTY3		PDA_ ERR2	PDA_ FULL_SYNC2	PDA_ EMPTY2
R/W	R	R	R	R	R	R	R	R
initial value	0	0	0	1	0	0	0	1
bit	7	6	5	4	3	2	1	0
reg		PDA_ ERR1	PDA_ FULL_SYNC1	PDA_ EMPTY1		PDA_ ERR0	PDA_ FULL_SYNC0	PDA_ EMPTY0
R/W	R	R	R	R	R	R	R	R
initial value	0	0	0	1	0	0	0	1

- PDA_ERR = PDA_ERROR

  Logical error in PDA. Error=1. Normally=0.

- PDA_FULL = PDA_FULL_SYNC

  Error to report that a buffer overflows in PDA. Error=1. Normally=0.

- P_EMPTY = PDA_EMPTY

  Error to report that a buffer becomes empty in PDA. Error=1. Normally=0.

2.2.10 RX_OVERFLOW_0/1/2/3 (8/9/10/11)

Counters which tell how many times FIFOs in RX0/1/2/3 have overflowed.

bit	7	6	5	4	3	2	1	0
reg	OVERFLOW_CNT							
R/W	R	R	R	R	R	R	R	R
initial value	0	0	0	0	0	0	0	0

- OVERFLOW_CNT

  Number of events in which FIFO in RX has overflowed. When a counter shows maximum 255 value, the counter keeps 255 value until it receives reset signal.

2.2.11 RX_FIFO_STATUS (12)

Checks errors in 4 RX at once.

And also reset values of FIFO overflow counters (RX_OVERFLOW_0/1/2/3).

bit								8
reg								FIFO_RST
R/W								R/W
initial value								0

bit	7	6	5	4	3	2	1	0
reg	FULL3	FULL2	FULL1	FULL0	EMPTY3	EMPTY2	EMPTY1	EMPTY0
R/W	R	R	R	R	R	R	R	R
initial value	0	0	0	0	1	1	1	1

- FIFO_RST

  Make FIFOs in all 4 RX be empty. These FIFOs is FIFOs showed in Figure 10, and is not either TP_FIFO or DMP_FIFO. Make empty=1. Don't make empty=0.

2.2.12 RX_RST (13)

Sends reset to each RX.

Positive logic. 1=reset. 0=initial value.

bit	3	2	1	0
reg	RST3	RST2	RST1	RST0
R/W	R/W	R/W	R/W	R/W
initial value	0	0	0	0

2.2.13 RX_CHANNEL_TO_SLEEP_ (14)

4 bit registers which can be read or written, but it is not implemented now.

bit	3	2	1	0
reg	SLEEP3_	SLEEP2_	SLEEP1_	SLEEP0_
R/W	R/W	R/W	R/W	R/W
initial value	1	1	1	1

2.2.14 RX_TP_WRITE (15)

Sets patterns of test data. When values are written in this register, values are directly copied to TP_FIFO. TP_FIFO is FIFO for test data.

bit	15	14	13	12	11	10	9	8
reg	TP_FULL	TP_EMPTY						
R/W	R	R	R	R	R	R	R	R
initial value	0	1	0	0	0	0	0	0
bit	7	6	5	4	3	2	1	0
reg				TP_PRV	TP_CUR	TP_NXT	TP_CTL	TP_FRAME_
R/W	R	R	R	W	W	W	W	W
initial value	0	0	0	0	0	0	0	0

- TP_FULL

  TP_FIFO has overflowed=1. Not overflowed=0.

- TP_EMPTY

  TP_FIFO is empty=1. TP_FIFO has data=0.

2.2.15 RX_TP_SETTING (16)

Sets to control test data.

bit	15	14	13	12	11	10	9	8
reg	TP_FULL	TP_EMPTY			TP_CH3	TP_CH2	TP_CH1	TP_CH0
R/W	R	R	R	R	R/W	R/W	R/W	R/W
initial value	0	1	0	0	0	0	0	0
bit	7	6	5	4	3	2	1	0
reg							TP_CLR	TP_START
R/W	R	R	R	R	R	R	R/W	R/W
initial value	0	0	0	0	0	0	0	0

- TP_START

  A command to send test data instead of SLB input data. start=1. Once test data mode is started, test data mode continues until TP_START is reset to be zero manually. When TP_START is one and data is written in RX_TP_WRITE, those data directly flows in RX.

- TP_CLR

  Resets TP_FIFO. TP_FIFO is forced to be empty. Reset=1. Don't reset=0.

- TP_CH

  Selects through which RX test data flows.(Select test data channels.) Flow test data=1. Flow SLB input data=0.
  When two or more channels are selected, same test patterns flow through selected channels at the same time.

2.2.16 RX_DMP_SETTING (17)

Sets dumping. It controls (start/clear) all 4 DMP_FIFOs at once.

bit	15	14	13	12	11	10	9	8
reg	DMP_FULL	DMP_EMPTY						
R/W	R	R	R	R	R	R	R	R
initial value	0	1	0	0	0	0	0	0
bit	7	6	5	4	3	2	1	0
reg							DMP_CLR	DMP_START
R/W	R	R	R	R	R	R	R/W	R/W
initial value	0	0	0	0	0	0	0	0

- DMP_START

  Selects whether input data fanned out are stored in DMP_FIFO or not. Start=1.
  Once dumping is started, DMP_FIFO continues to dump data until DMP_FIFO overflows.

- DMP_CLR

  A command to make DMP_FIFO empty. Make empty=1.

2.2.17 RX_DMP_READ_0/1/2/3 (18/19/20/21)

Reads values per 1 clock in DMP_FIFO.

There is one DMP_FIFO against each RX. Data can be read out from each DMP_FIFO.

bit	15	14	13	12	11	10	9	8
reg	DMP_FULL	DMP_EMPTY						
R/W	R	R	R	R	R	R	R	R
initial value	0	1	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
reg				DMP_PRV	DMP_CUR	DMP_NXT	DMP_CTL	DMP_FRAME_
R/W	R	R	R	R	R	R	R	R
initial value	0	0	0	0	0	0	0	0

- DMP_FULL

  When one of 4 DMP_FIFOs becomes full, DMP_FULL=1. When all 4 DMP_FIFOs are not full, DMP_FULL=0. (OR of 4 FIFO_FULL)

- DMP_EMPTY

  When all 4 DMP_FIFOs are empty, DMP_EMPTY=1. When one of 4 DMP_FIFOs has some data, DMP_EMPTY=0. (AND of 4 FIFO_EMPTY)

2.3 TX VME Registers

2.3.1 Register Table

The VME register map of TX_FPGA is shown and explained below.

TX_TIME_TO_WAIT, TX_TIME_TO_WAIT2, TX_EDGE_SEL, TX_MASK_NEW, TX_GL_STAT, TX_TP_SETTING, TX_DMP_SETTING are implemented using voting logic structure.

When undefined addresses (from 16 to 31) are read, the value 0xcdef will be returned. (0xcdef is 1100_1101_1110_1111 as a binary number.)

address	register name	R/W	initial value	size
Initial settings				
0	TX_READ_SSWID	R/W	00_1111	6
1	TX_TIME_TO_WAIT	R/W	1111_1111	8
2	TX_TIME_TO_WAIT2	R/W	1_1111_1111	9
3	TX_EDGE_SEL	R/W	111	3
Masks				
4	TX_MASK_NEW_L_	R/W	0000_0000_0000	12
5	TX_MASK_NEW_H_	R/W	000_0000_0000	11
6	TX_MASK_CUR_L_	R	0000_0000_0000	12
7	TX_MASK_CUR_H_	R	000_0000_0000	11
Optical signaling(Glink)				
8	TX_GL_STAT	R/W	00	2
Error checks				
9	TX_ERRORS0	R	0000_0000_0000_0000	16
10	TX_ERRORS1	R	0000_0000_0000_0000	16
Test patterns				
11	TX_TP_WRITE_L	R/W	0000_0000_0000_0000	16
12	TX_TP_WRITE_H	R/W	0000_0000_0000_0000	16
13	TX_TP_SETTING	R/W	0000	4
Dumps				
14	TX_DMP_SETTING	R/W	0000_0000_0000_0000	16
15	TX_DMP_READ	R	0000_0000_0000_0000	16

2.3.2 TX_READ_SSWID (0)

Checks both SSWID and REC_TYPE. SSWID is set at dip-switch. REC_TYPE is unchangeably written within FPGA. (Now REC_TYPE is set to be zero.)

bit	5	4	3	2	1	0
reg	REC_TYPE1	REC_TYPE0	SSWID3	SSWID2	SSWID1	SSWID0
R/W	R	R	R	R	R	R
initial value	0	0	1	1	1	1

- REC_TYPE

  Record Type. It is a version number of FElink format. When FPGA design is revised and data format changes, SSW reports this revision to ROD by REC_TYPE value.

2.3.3 TX_TIME_TO_WAIT (1)

Time which TX can spend in reading 1 event data from up to 23 RX. Data which comes after TX_TIME_TO_WAIT clocks are not read out and given up. TX_TIME_TO_WAIT can be set up to 255 clocks.

bit	7	6	5	4	3	2	1	0
reg	TIME_TO_WAIT							
R/W	R/W							
initial value	8'd255							

2.3.4 TX_TIME_TO_WAIT2 (2)

Time which TX can spend in reading data from 1 RX. Data which comes after TX_TIME_TO_WAIT clocks are not read out and given up. TX_TIME_TO_WAIT2 can be set up to 511 clocks.

bit	8	7	6	5	4	3	2	1	0
reg	TIME_TO_WAIT2								
R/W	R/W								
initial value	9'd511								

2.3.5 TX_EDGE_SEL (3)

Selects whether TX receives/sends data at the positive edge of the clock or the negative edge of the clock.

bit	2	1	0
reg	EDG_GL	EDG_BUS1	EDG_BUS0
R/W	R/W	R/W	R/W
initial value	1	1	1

- EDG_GL

  Indicates whether SSW TX sends data to a Glink serializer at the positive edge (posedge) or the negative edge (negedge) of clock. Posedge=1. Negedge=0.

- EDG_BUS

  Indicates whether TX FPGA receives data from RX FPGAs at posedge or negedge of the clock. Posedge=1. Negedge=0.
  EDG_BUS1 is a setting for 18 dbus lines, and EDG_BUS1 is a setting for 23 lines which report FIFO empty.

2.3.6 TX_MASK_NEW_L_ (4)

New setting of masks against RXs. TX_MASK_NEW_L_ set the mask from RX11 to RX0.

bit					11	10	9	8
reg					MN11_	MN10_	MN9_	MN8_
R/W					R/W	R/W	R/W	R/W
initial value					0	0	0	0
bit	7	6	5	4	3	2	1	0
reg	MN7_	MN6_	MN5_	MN4_	MN3_	MN2_	MN1_	MN0_
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
initial value	0	0	0	0	0	0	0	0

- MN_ = MASK_NEW_

  Sets a mask against each RX. TX ignores masked RXs. Mask=0. Don't mask=1.

2.3.7 TX_MASK_NEW_H_

New setting of masks against RXs. TX_MASK_NEW_L_ set the mask from RX22 to RX12.

bit						10	9	8
reg						MN22_	MN21_	MN20_
R/W						R/W	R/W	R/W
initial value						0	0	0

bit	7	6	5	4	3	2	1	0
reg	MN19_	MN18_	MN17_	MN16_	MN15_	MN14_	MN13_	MN12_
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
initial value	0	0	0	0	0	0	0	0

2.3.8 TX_MASK_CUR_L_ (6)

Returns the current setting value of the masks against RXs. TX_MASK_NEW_L_ shows the mask from RX11 to RX0.

Mask setting are updated with values of TX_MASK_NEW_L/H_ only when all RX are IDLE state and TX isn't reading data.

bit					11	10	9	8
reg					MC11_	MC10_	MC9_	MC8_
R/W					R	R	R	R
initial value					0	0	0	0

bit	7	6	5	4	3	2	1	0
reg	MC7_	MC6_	MC5_	MC4_	MC3_	MC2_	MC1_	MC0_
R/W	R	R	R	R	R	R	R	R
initial value	0	0	0	0	0	0	0	0

- MC_ = MASK_CUR_

  Sets a mask against each RX. TX ignores masked RXs. Mask=0. Don't mask=1.

2.3.9 TX_MASK_CUR_H_ (7)

Returns the current setting value of the masks against RXs. TX_MASK_NEW_L_ shows the mask from RX22 to RX12.

bit						10	9	8
reg						MC22_	MC21_	MC20_
R/W						R	R	R
initial value						0	0	0

bit	7	6	5	4	3	2	1	0
reg	MC19_	MC18_	MC17_	MC16_	MC15_	MC14_	MC13_	MC12_
R/W	R	R	R	R	R	R	R	R
initial value	0	0	0	0	0	0	0	0

2.3.10 TX_GL_STAT (8)

Shows link state of Glink signaling.

bit	1	0
reg	GL_LOCK	GL_IDLE
R/W	R	R/W
initial value	0	0

- GL_LOCK

  Shows link state of Glink. Lock=1. Unlock=0.

- GL_IDLE

  A command to make Glink's TXCNTL and TXDATA pins low and to force Glink serializer to output idle word. Output idle word=1. Don't output idle word=0.

2.3.11 TX_ERRORS0 (9)

Checks values of error counters in stage1_buffer and analyzing_sequencer.

bit	15	14	13	12	11	10	9	8
reg	DATABUF_OVERFLOW_COUNT				ADDRESS_SEQUENCE_ERROR_IN_COUNT			
R/W	R				R			
initial value	0				0			

bit	7	6	5	4	3	2	1	0
reg	ADDRESS_SEQUENCE_ERROR_OUT_COUNT				ANALYSIS_ERROR_COUNT			
R/W	R				R			
initial value	0				0			

- DATABUF_OVERFLOW_COUNT

  This value tells how many times FIFO in stage1_buffer has overflowed.
  Once ADDR_ERRORS0 is read, this value is reset to zero.

- ADDRESS_SEQUENCE_ERROR_IN_COUNT

  This value tells how many times the order of cell_address of stage1_buffer's input data has collapsed.
  Once ADDR_ERRORS0 is read or receives reset signals, this value is reset to zero.

- ADDRESS_SEQUENCE_ERROR_OUT_COUNT

  This value tells how many times the order of cell_address of stage1_buffer's input data has collapsed.
  Once ADDR_ERRORS0 is read or receives reset signals, this value is reset to zero.

- ANALYSIS_ERROR_COUNT

  This value tells how many times inconsistency has happened between analyzing_sequencer state and tags of input data.
  Once ADDR_ERRORS0 is read or receives reset signals, this value is reset to zero.

2.3.12 TX_ERRORS1 (10)

Checks values of error counters in stage1_buffer and bus_controller.

bit	15	14	13	12	11	10	9	8
reg	RST_DATABUF_ERROR	DATABUF_STATUS			CS_ERROR_COUNT			
R/W	R	R			R			
initial value	0	0			0			

bit	7	6	5	4	3	2	1	0
reg	NORES_COUNT				TIMEOUT2_COUNT			
R/W	R				R			
initial value	0				0			

- RST_DATABUF_ERROR

  An error which tells that stage1_buffer receives next event data before stage1_buffer become empty. Error=1.

- DATABUF_STATUS

This value tells how many bits waddr has precede raddr at a maximum by, or what amount of data has stored in FIFO.
Once ADDR_ERRORS1 is read or receives reset signals, this value is reset to zero.

- CS_ERROR_COUNT

This value tells how many times bus_controller has selected two or more RX at once.
Once ADDR_ERRORS1 is read or receives reset signals, this value is reset to zero.

- NORES_COUNT

This value tells in how many events there are RXs which are not masked but stay empty after TIME_TO_WAIT passed. (RX like this are called No-Response RX.)
Once ADDR_ERRORS1 is read or receives reset signals, this value is reset to zero.

- TIMEOUT2_COUNT

This value tells how many times TX can't read data trailer after TIME_TO_WAIT2 passed. Once ADDR_ERRORS1 is read or receives reset signals, this value is reset to zero.

2.3.13 TX_TP_WRITE_L (11)

Sets lower 16 bits ([15:0]) of test data patterns.
Whole size of registers for test data patterns is 32 bits.

bit	15	14	13	12	11	10	9	8
reg	TP15	TP14	TP13	TP12	TP11	TP10	TP9	TP8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
initial value	0	0	0	0	0	0	0	0
bit	7	6	5	4	3	2	1	0
reg	TP7	TP6	TP5	TP4	TP3	TP2	TP1	TP0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
initial value	0	0	0	0	0	0	0	0

2.3.14 TX_TP_WRITE_H (12)

Sets upper 16 bits ([31:16]) of test data patterns.

bit	15	14	13	12	11	10	9	8
reg	TP31	TP30	TP29	TP28	TP27	TP26	TP25	TP24
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
initial value	0	0	0	0	0	0	0	0
bit	7	6	5	4	3	2	1	0
reg	TP23	TP22	TP21	TP20	TP19	TP18	TP17	TP16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
initial value	0	0	0	0	0	0	0	0

2.3.15 TX_TP_SETTING (13)

A command to control (start/clear) test data. Glink control-word in test data is set at once.

Because test patterns are stored not in FIFO but in registers, start instruction can be done continuously.

bit	3	2	1	0
reg	TP_HEAD1	TP_HEAD0	TP_CLR	TP_START
R/W	R/W	R/W	R/W	R/W
initial value	0	0	0	0

- TP_START

  A command to send test pattern in stead of TX output data. Send test pattern=1. Send TX output data=0.
  Once test patterns are started, patterns in
  TX_TP_WRITE_H and TX_TP_WRITE_L are sent in 2 consecutive clocks.

- TP_CLR

  A command to clear 32 bits values in both TX_TP_PATTERN_L and TX_TP_PATTERN_H. Clear=1.

- TP_HEAD0/1

  Glink header word with which test patterns are identified as control-word or data-word. Data are added these 2 bits and send to Glink serializer.

2.3.16 TX_DMP_SETTING (14)

Sets dumping.

bit	15	14	13	12	11	10	9	8
reg	DMP_FULL	DMP_EMPTY						
R/W	R	R	R	R	R	R	R	R
initial value	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
reg						DMP_NOIDLE	DMP_CLR	DMP_START
R/W	R	R	R	R	R	R/W	R/W	R/W
initial value	0	0	0	0	0	0	0	0

- DMP_START

  Selects whether TX output data fanned out are stored in DMP_FIFO or not. Start=1. Don't start=0.

- DMP_CLR

  Clears values in DMP_FIFO. Clear=1.

- DMP_NOIDLE

  Selects whether Glink IDLE word may be stored in DMP_FIFO or not. Don't store IDLE word=1. Store IDLE word=0.

- DMP_FULL

  When DMP_FIFO becomes full, DMP_FULL=1. When DMP_FIFO doesn't become full, DMP_FULL=0.

- DMP_EMPTY

  When DMP_FIFO becomes empty, DMP_EMPTY=1. When DMP_FIFO has some data, DMP_FIFO=0.

2.3.17 TX_DMP_READ (15)

Reads values from DMP_FIFO.

bit	15	14	13	12	11	10	9	8
reg	DMP15	DMP14	DMP13	DMP12	DMP11	DMP10	DMP9	DMP8
R/W	R	R	R	R	R	R	R	R
initial value	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
reg	DMP7	DMP6	DMP5	DMP4	DMP3	DMP2	DMP1	DMP0
R/W	R	R	R	R	R	R	R	R
initial value	0	0	0	0	0	0	0	0