JLC Trigger and DAQ

Presented at the 4th International Workshop on Linear Colliders
May 3, Sitges, Barcelona, Spain

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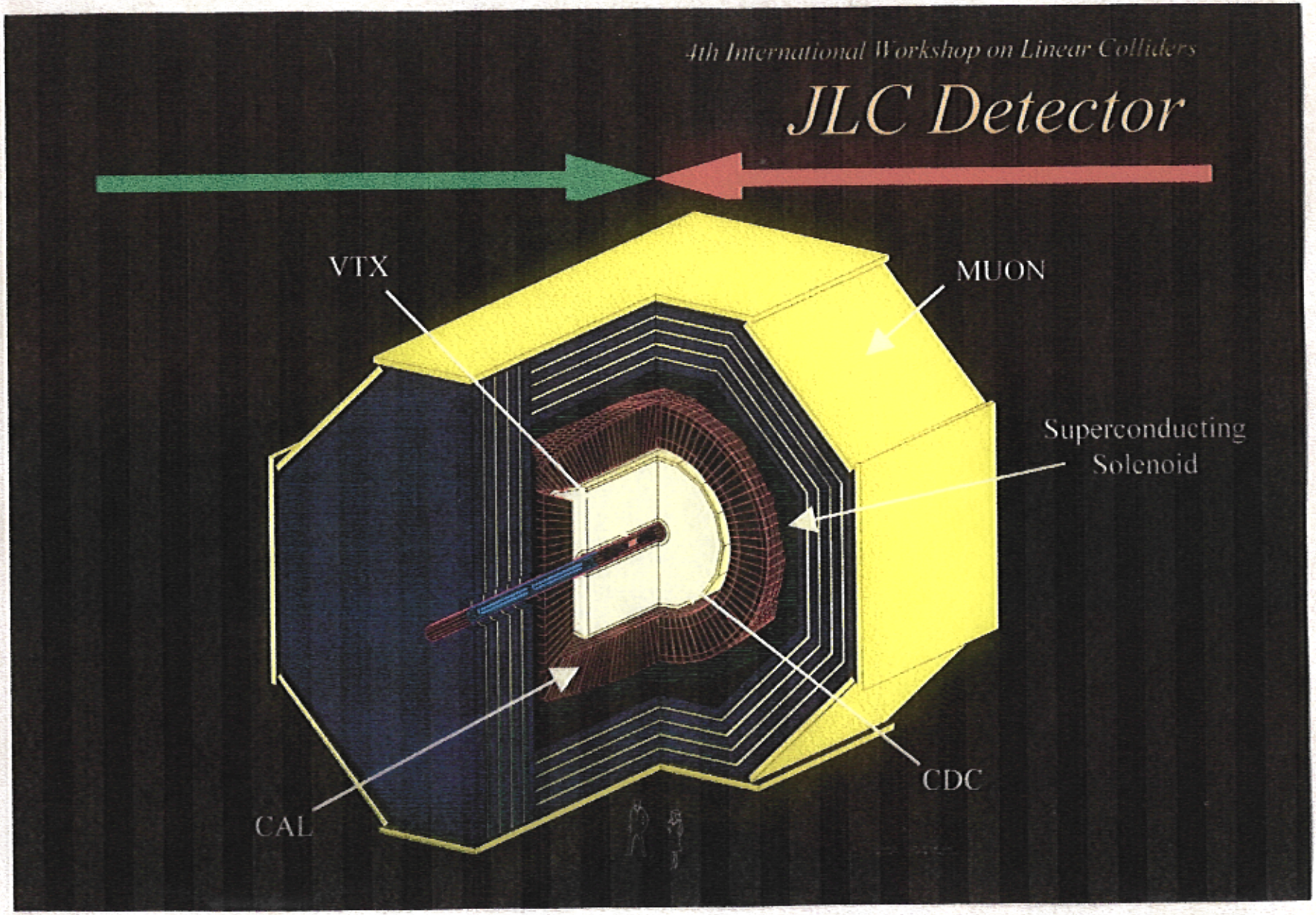
4th International Workshop on Linear Colliders
JLC Detector
VTX
MUON
Superconducting
Solenoid
CDC
CAL

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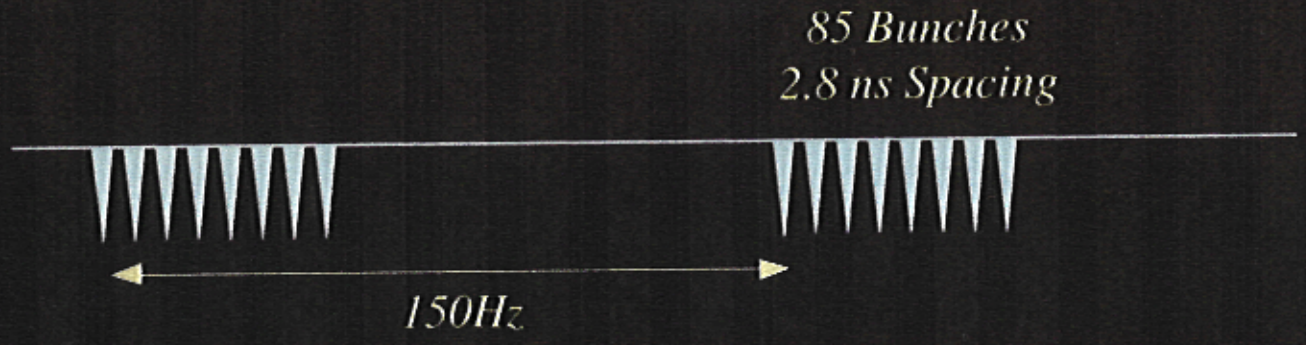
JLC Detector Parameters

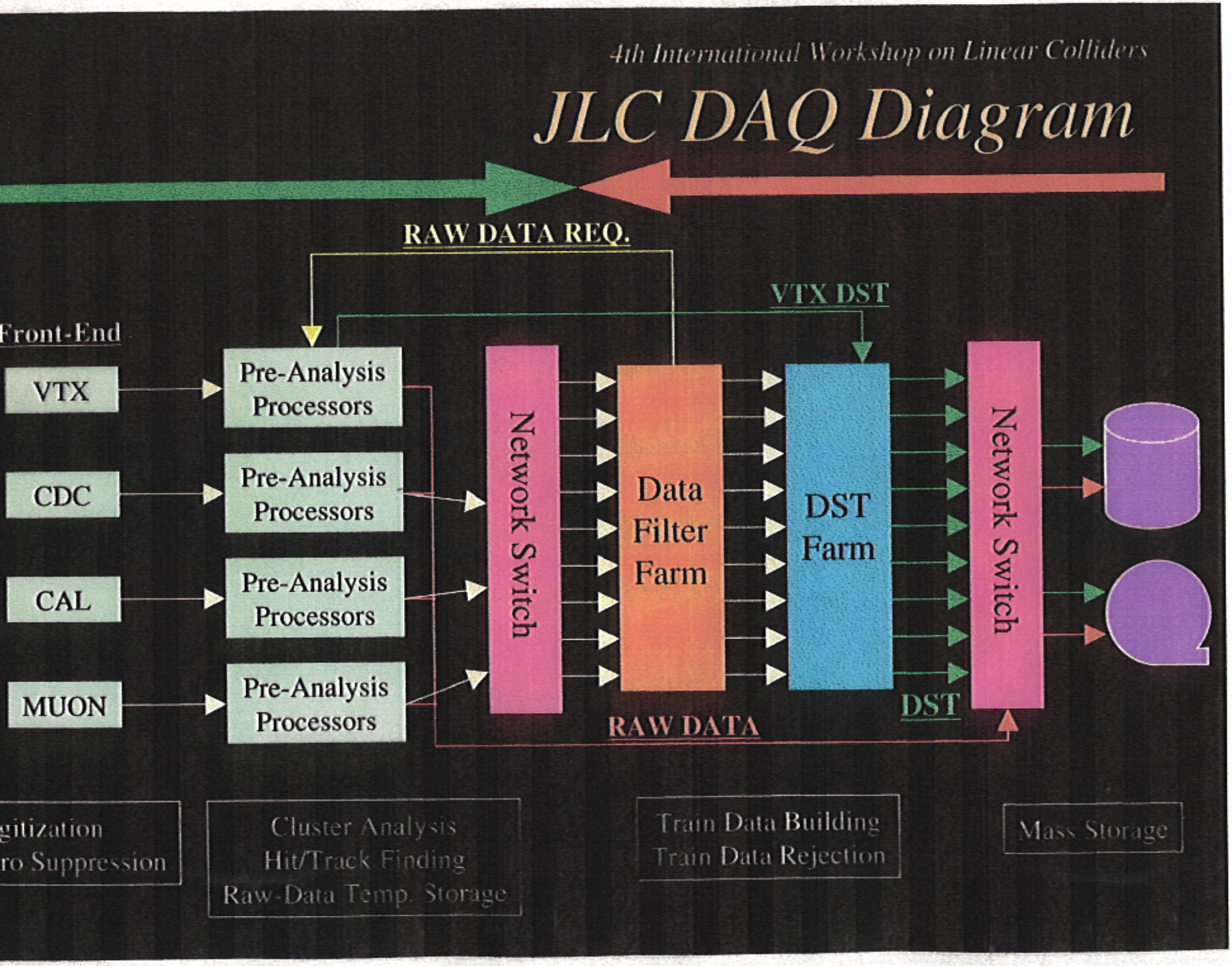
Detector	Type	Configuration / Read-out		Performance
VTX	Silicon CCD	Pixel size: 25μm Number of layers: 4 Layer position: 2.4/3.6/4.8/6.0cm Thickness: 200μm/layer $\|\cos\theta\| < 0.9$		Position resolution: $\sigma = 4\mu m$ Impact parameter resolution δ(μm): $\delta^2 = 7^2 + (20.0/p)^2/\sin^3\theta$
CDC	Small-cell Jet Chamber	Radius: 0.4~2.3m Length: 4.6m Number of sampling: 86 $\|\cos\theta\| < 0.70$ (Full sampling) $\|\cos\theta\| < 0.95$ (20 sampling)		Position resolution: σ_x = 86μm (by axial wires) σ_z = 2mm (by stereo wires) Momentum resolution: $\sigma_{Pt} = 1.1 \times 10^{-3}$ Pt ⊕ 0.1% $\sigma_{Pt} = 5 \times 10^{-3}$ Pt ⊕ 0.1% with vertex constraint
CAL	Lead + Plastic Scintillator Sandwich (Compensated)	EM	Thickness: $29X_0$ Cell size: 10cm × 10cm	Energy resolution: $\sigma_E / E = 15\% / \sqrt{E} \oplus 1\%$ (e & γ) $\sigma_E / E = 40\% / \sqrt{E} \oplus 2\%$ (Hadron)
		HAD	Thickness: $5.6\lambda_0$ Cell size: 20cm × 20cm Longitudinal segment: 2 segments	
		Si pad	Pad size: 1cm × 1cm	
		$\|\cos\theta\| < 0.9$		
MUON	TGC + RPC + Drift Chamber (?)	Number of superlayers: 5 $\|\cos\theta\| < 0.99$		Position resolution: ~ mm Pt > 2.2GeV/c: Reach return yoke Pt > 5.2GeV/c: Penetrate return yoke

Basic Concepts

- JLC Beam Structure



  - No Hardware Trigger Logic
  - DAQ Triggered by Every Train Crossing
  - Bunch ID provided by Off-line Analysis
    - CAL Timing & CDC T0 Fitting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JLC DAQ Diagram
RAW DATA REQ.
VTX DST
Front-End
VTX
CDC
CAL
MUON
Pre-Analysis Processors
Pre-Analysis Processors
Pre-Analysis Processors
Pre-Analysis Processors
Network Switch
Data Filter Farm
DST Farm
Network Switch
DST
RAW DATA
gitization
ro Suppression
Cluster Analysis
Hit/Track Finding
Raw-Data Temp. Storage
Train Data Building
Train Data Rejection
Mass Storage

Data Read-out

- DAQ Repetition Rate @ 150Hz
- Digitization, Zero Suppression in the Frond-End Electronics
- Dead-Time Free

Subsystems	Channel Count		Typical Data Size (bytes)
	Total	One Event	
VTX	320M	360K	1.4M
CDC	17M	3M	12M
CAL	2.1M	7.8K	32K
MUON	TBD	TBD	TBD
Total	340M	3.4M	13.5M

VTX Reaa-out

- CCD VTX
  - 4 Layers (R = 2.4/3.6/4.8/6.0 cm), $|\cos\theta| < 0.9$
  - 25mm×5mm CCD Pad (200K 25μm□ Pixels/Pad)
  - 1600 CCD Pads (~ 320M Pixels)
  - FADC Read-out @ Each CCD Pad
    - Read-out Time 4 ms @ 50 MHz Sampling
      20 ms @ 10 MHz Sampling
  - 40 K Hits/Train including Noise/BG Tracks
  - Zero Suppression (3×3 Pixels around Peak)
    - 4 bytes/Pixel → 1.4 Mbytes/Train

CDC Reaa-out

- Small-Cell Jet-Chamber
  - 1200 Cells, 7-Sense Wires/Cell
  - 17 K FADC Channels (Both End of a Wire)
  - 200 MHz 12-bit Sampling
    - Full Drift ~ 5μs (=Read-out Time)
    - 100 Time-Slice (500 ns)/Hit by Zero Suppression
  - 30 K Hits/Train including Mini-jet Background
    - 4 bytes/Time-Slice → 12 Mbytes/Train

CAL Reaa-out

- Lead-Plastic Scintillator Sandwich
  - ECAL 10 cm□ 20 K Channels
  - HCAL 20 cm□× 2 Segments 10 K Channels
  - Silicon Pad 1 cm□ 2 M Channels
- 12-bit ADC Read-out
  - 100 μs Data Conversion
  - Multiplexed Read-out for Si Pads
- Zero Suppression
  - 2 K Data for ECAL, 0.6 K Data for HCAL
  - 6 K Data for Silicon Pads
  - 4 bytes/Hits → 32 Kbytes/Train

Data Reauction

- 3-stage Data Reduction
  - Pre-Analysis Processors
    - Installed in Each Sub-detector
    - Hardware Sequencer or Software Processing
    - Provide Cluster/Hit/Track to Data Filter Farm
    - Temporary Storage Buffer of Raw-Data

    - Expected Data Size to Data Filter ~ 1/10 of Raw Data
      - 100 Time-Slices/Hit in CDC
        → Several Words (Time-Stamp/Charge...)
      - Sum-up ADC Value in a Cluster in ECAL/HCAL

- Data Filter Farm
  - Multiple CPU Complex
  - Reject Data containing ONLY Mini-Jet Background based on CDC/CAL Track/Cluster Information
    - Number of High P_t Tracks in CDC (Fast Track Recognition)
    - Total or Segmented Energy Flow in CAL
    - VTX Information is NOT Available (Slow Read-out)
  - Expected Rejection Factor
    - 10~20 @ $\sqrt{s}$ = 0.5 ~ 1.5 TeV
    - No Rejection @ Z^0 Peak
      - Every Train contain "Physics Processes"

- Decision in a few milliseconds should be Required
  - Accept :
    - Send VETO Signal to LINAC to Stop Next Beam Train Crossing to Avoid Multiple Train Overlapping in VTX
    - Request DST Farm to Build DST
    - Request Pre-Analysis Processors to Sending Raw-Data
  - Reject :
    - Clear Frond-End Electronics and Pre-Analysis Processors
    - VTX Needs 1 ms to Clear CCD

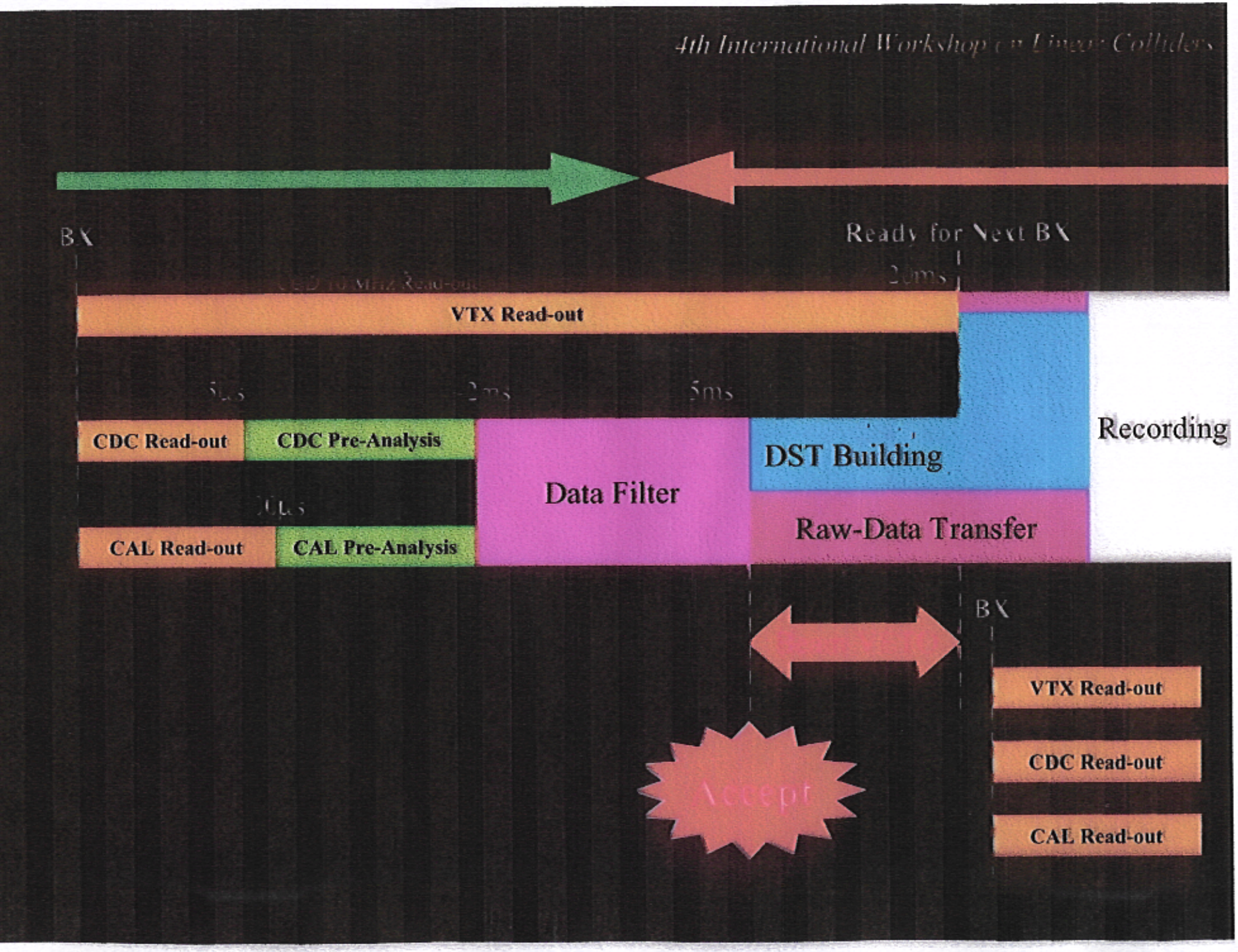
- On-line DST Production
  - Multiple CPU Complex
  - DST Contains
    - VTX Cluster, CDC Hit, CAL Cluster… From Pre-Analysis
    - CDC Track, Energy Flow in CAL … From Data Filter
  - Data Size of DST ~ 1 Mbytes/Train
  - Seriously Required for DAQ @ Z^0 Peak
    - No Rejection by Data Filter
    - Limited Data Recording Speed
      - → Give-up Raw-Data Recording ???

Data Recording

- Raw Data Recording @ $\sqrt{s}$ = 0.5 ~ 1.5 TeV
  - 12 Mbytes, ~10 Hz → 120MB/s
- On-line DST Recording @ Z^0 Peak
  - 1 Mbytes, 150 Hz → 150 MB/s

→ 10 Tbytes / Day

→Further Reduction may be Required for Permanent Storage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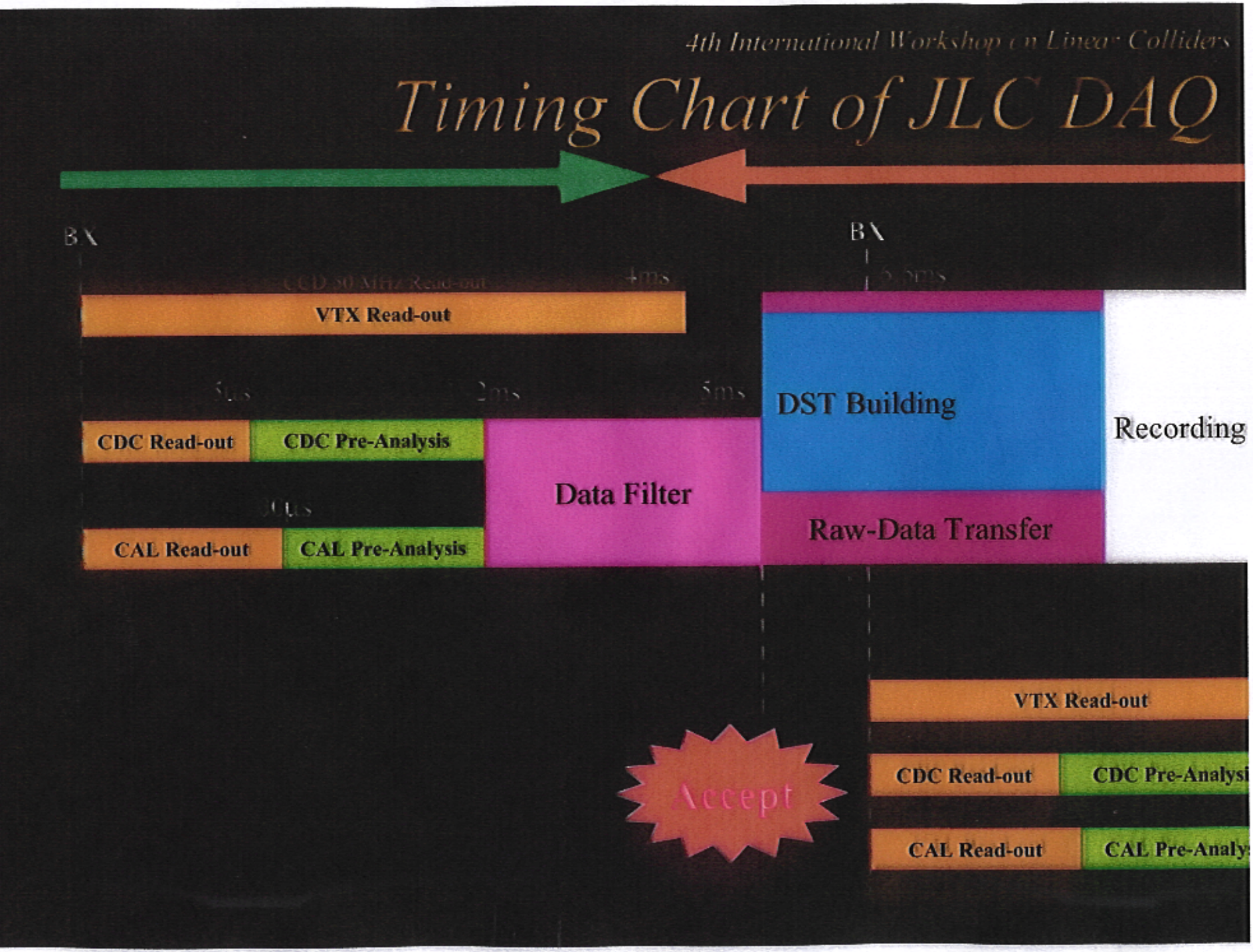
BX
Ready for Next BX
20ms
VTX Read-out
2ms
5ms
CDC Read-out
CDC Pre-Analysis
CAL Read-out
CAL Pre-Analysis
Data Filter
DST Building
Raw-Data Transfer
Recording
BX
Accept
VTX Read-out
CDC Read-out
CAL Read-out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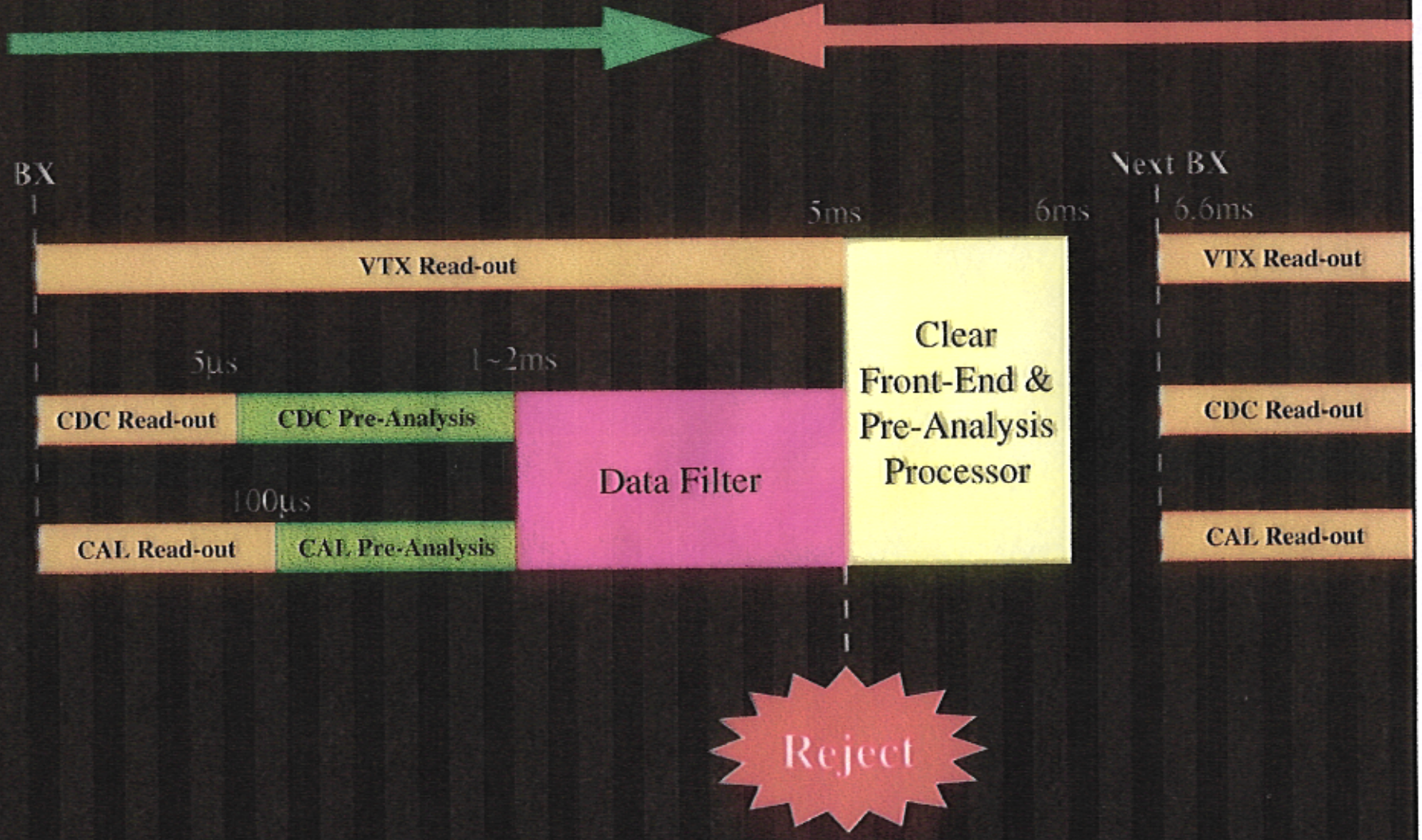
Timing Chart of JLC DAQ
BX
BX
VTX Read-out
DST Building
Recording
CDC Read-out
CDC Pre-Analysis
Data Filter
CAL Read-out
CAL Pre-Analysis
Raw-Data Transfer
Accept
VTX Read-out
CDC Read-out
CDC Pre-Analysi
CAL Read-out
CAL Pre-Analy


BX
Next BX
5ms
6ms
6.6ms
VTX Read-out
VTX Read-out
5μs
1~2ms
CDC Read-out
CDC Pre-Analysis
CDC Read-out
Data Filter
Clear
Front-End &
Pre-Analysis
Processor
100μs
CAL Read-out
CAL Pre-Analysis
CAL Read-out
Reject

Available Technologies

- Data Transfer
  - Gbps Network (ATM, FCS ....)
  - Switches > 10 Gbps Bandwidth
- Processors
  - 10^5 MIPS, SMP Technology
- Mass Storage System
  - 100 Mbytes/s for Single HDD (FC-AL)
  - 64 Mbytes/s for Single ID-1 Tape Drive
  - TBytes Disk Array & PBytes Tape System

Milestones

- Fall 1999
  - Fix No. of Read-out Channels and Data Size
- Spring 2000
  - Complete Conceptual Design of DAQ System
- Fall 2000
  - Complete Technical Design
  - Cost Estimation based on Current Technologies